FINAL PROGRAM REPORT
FOR
DEVELOPMENT OF RESONANT TUNNELING DIODE CIRCUITS USING EPITAXIAL LIFTOFF

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The program was to determine the potential perfomance advantages of integrating resonant tunneling diodes (RTDs) with complementary metal oxide semiconductor (CMOS) technology. In this program, a broad suite of circuits was fabricated and evaluated for logic memory, optoelectronic, and mixed-signal applications. We conclude that mixed-signal RT-CMOS circuits have performance advantages for niche applications in t;he short term, and broad use in logic when silicon-based RT technology reaches production maturity.

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LIST OF ACRONYMS

A/D	Analog-to-Digital (Converter)
BCB	Benzocyclobutene
CMOS	Complementary Metal Oxide Semiconductor
ELO	Epitaxial Liftoff (Method)
FOX	Flowable Oxide
FET	Field Effect Transistor
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
InP	Indium Phosphide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSIS	An integrated circuit fabrication service provided by USC/ISI
PECVD	Plasma-Enhanced Chemical Vapor Deposition
QMOS	Quantum Metal Oxide Semiconductor (term coined at Raytheon to identify MOS circuits that have been augmented with RT devices)
PVR	Peak-to-Valley Current Ratio
RIE	Reactive Ion Etching
RT	Resonant Tunneling
RTD	Resonant Tunneling Diode
S-parameter	Scattering Parameter
SPICE	Simulation Program With Integrated Circuit Emphasis
TiW	Titanium Tungsten
USC/ISI	University of Southern California Information Sciences Institute
III-V	Semiconductor compounds of Groups III and V of the Periodic Table of the Elements (e.g., GaAs)

ACKNOWLEDGMENTS

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The ELO Project Team

EXECUTIVE SUMMARY

The overall objective of this program was to determine the potential performance advantages of integrating resonant tunneling diodes (RTDs) with complementary metal oxide semiconductor (CMOS) technology. Historically, RT technology has been developed in Groups III-V semiconductors on gallium arsenide (GaAs) and indium phosphide (InP) substrates. Silicon-based RTDs are relatively undeveloped, so it was infeasible in 1996 to develop epitaxial, monolithic RT-CMOS integrated circuits. For this reason, RT-CMOS technology was explored using a novel transferred substrate method that mechanically integrated InP RTDs with CMOS circuitry. This fusion of III-V and silicon devices and processes allowed an "early look" at the potential for quantum devices to reduce power consumption and increase functional density in mainstream silicon technology. The hybrid integration approach also offers the possibility of developing small RT-CMOS integrated circuits for custom applications that are not well served by either material system alone. As epitaxial growth technology matures, it will be feasible to integrate RT devices with conventional CMOS technology.

In this program, a broad suite of circuits was fabricated and evaluated for logic, memory, optoelectronic, and mixed-signal applications. In general, we found that the class of mixed-signal circuits such as analog-to-digital (A/D) converters is best-suited to hybrid RTD-CMOS technology. These circuits can offer significant improvement over all-CMOS designs in terms of speed-power product, due to the RTD's inherently high switching speed and extrinsic bistability. Because of the relatively large sizes of the devices and interconnects used in the transferred substrate process, we did not observe a major speed improvement in comparison to that of the best dynamic CMOS logic designs. Based on computer simulations, however, a truly monolithic (that is, epitaxial) RTD/CMOS technology would provide a significant improvement in speed and power efficiency for logic functions.

We conclude that mixed-signal RT-CMOS circuits have performance advantages for niche applications in the short term, and broad use in logic when silicon-based RT technology reaches production maturity.

1. INTRODUCTION

This final report summarizes the technical progress made under Contract No. F49620-96-C-0050, as required in CLIN 0002AB of the agreement.

1.1 Goals

The overall objective of this program was to determine the potential advantages of nanoelectronic resonant tunneling (RT) devices when integrated with CMOS technology. This section summarizes the specific design and fabrication goals of the program.

Circuit Design Goals

- Simulate basic logic elements using available CMOS and RTD process models in SPICE.
- Design novel RTD-CMOS circuits compatible with InP-based RTDs available from Raytheon Systems and the CMOS integrated circuit processes available from the MOSIS foundry.
- Simulate competitive all-CMOS equivalents for each RTD-CMOS circuit. These baseline simulations would form the foundation for comparison between CMOS and hybrid RTD-CMOS designs. The comparison gave upper bounds on the relative performance of the RTD-CMOS designs.
- Adapt existing designs from the QMOS program to the circuit and layout requirements necessary for RTD-CMOS thin-film integration.
- Simulate circuit designs and optimize to account for the parasitics associated with the thin-film integration process.

Process Development Goals

- Grow and fabricate RTDs with required DC characteristics. Based on CMOS and RTD simulations, grow with molecular beam epitaxy the RTDs with current-voltage characteristics that are best suited to the RTD-CMOS circuit designs.

- Improve the RTD substrate transfer process. Initial research demonstrated that single RTDs could be removed from their InP growth substrate and transferred to a new host substrate without degrading their DC characteristics. A process was to be developed that allows for lateral placement of an InP-based RTD structure onto a silicon CMOS circuit, as well as electrically interconnecting the RTD to an arbitrary circuit. This is to be done with minimal degradation in the RTD performance.

- Improve interconnection techniques. Since the performance of the RTD-CMOS circuits is limited by circuit parasitics, the interconnection process is critical. This need was to be addressed by improving and scaling the interconnection between the RTD and the CMOS circuit.

- Develop fabrication processes to allow for integration of multiple RTDs onto silicon circuits. To benchmark more advanced RTD-CMOS circuits, techniques to create circuits with multiple RTDs needed to be perfected. This required improvement of both the RTD fabrication and the thin-film integration process.

Circuit Characterization

- Measure DC operating characteristics to demonstrate circuit function. Fabricated CMOS and RTD-CMOS circuits were to be measured and compared in terms of power dissipation and functional density. Measurements also were to be checked against SPICE simulation.

- Measure high-speed circuit performance. CMOS and RTD-CMOS circuits were to be measured in terms of power dissipation and speed.

Evaluation of the Limits of RTD-CMOS Circuits

- Evaluate the performance limitations of RTD-CMOS circuits, both analog and digital, and find the circuit topologies where RTD-CMOS circuits offer the greatest advantage over all-CMOS circuits in either speed or power consumption.

- Evaluate the performance limits of the thin-film integration process as it relates to RTD-CMOS hybrid integration.

1.2 Accomplishment Summary

All of the major program goals in design, process development, fabrication, and characterization were accomplished. This section highlights our progress in these areas.

Circuit Design and Simulation

- Designs from the concurrent QMOS program (Contract No. F49620-96-C-0006) were adapted to MOSIS 0.5 μm CMOS technology and existing InP-based RTDs from Raytheon Systems. These digital circuits included: static-2NAND, bistable 2NOR, clocked inverter, shift register, edge-triggered flip-flop, and a bistable half-adder (carry and sum circuits).

- Novel RTD-CMOS logic and memory elements were designed for implementation with a single RTD: a multistate SRAM, a three-input majority gate, and an RTD-CMOS XOR. These circuits demonstrated the wide range of circuits that can be implemented in an integrated RTD-CMOS technology. In addition, two-RTD binary tunneling SRAMs were simulated that show the potential for reduced power consumption in relation to standard all-CMOS designs.

- RTD-CMOS comparators were designed for implementation in RTD-CMOS integrated circuits. Both clocked and self-resetting versions were designed.

- IC layout conventions were developed for integrating CMOS circuits with thin-film devices.

Process Development

- A thin-film integration process was developed for the integration of InP RTDs with foundry CMOS circuits. Excellent lateral alignment was achieved, which allowed reliable integration of RTDs with prefabricated CMOS integrated circuits after some pre-transfer processing on the CMOS chip. This process showed little or no degradation of the pre-transfer RTD characteristics. Experiments on InP HBTs showed that the thin-film integration method can be extended to integrate three-terminal devices and perhaps high-speed InP-circuits onto silicon circuitry.

- An improved RTD fabrication process was developed to optimize the thin film RTD structures. Reduced parasitic capacitance was achieved by scaling the RTDs down in size and using an advanced interlayer dielectric process. These structures were planarized to allow for topside-only contacts. This development allowed for simplified pre-processing of the CMOS circuit along with integration of multi-RTD structures onto circuits with no increase in processing time or modification of the integration process. Frontside-only RTDs were successfully transferred to silicon with no change in RTD characteristics.

- Improved interconnection techniques were developed for advanced RTD-structures. Specifically, this technique used a thick (3 to 5 μm) organic dielectric to separate the interconnects to the RTD from the conductive, lossy silicon substrate of the CMOS chip. This integration technique allowed both terminals to the RTDs to be connected with low parasitic capacitance. This is a dramatic improvement over our initial thin-film integration technique that allowed for only one low parasitic interconnect.

Circuit Characterization

Several RTD-CMOS circuits were demonstrated, including RTD-CMOS comparators, a Schmitt inverter, and a transimpedance amplifier. All circuits performed as simulated. These circuits could not be accurately benchmarked against their CMOS equivalents because of the pad parasitics associated with thin-film integration and the high currents of the RTDs.

Limits of Thin Film Integration and RTD-CMOS Circuits

- Of the circuit concepts studied, it was found that the class of circuits best-suited to RTD-CMOS technology is the comparator, which forms the basis of analog-to-digital converter circuits. These circuits offer significant improvement over all-CMOS designs in a given process technology, in terms of speed-power product, due to the RTD's inherently high switching speed and bistable operation.

- In developing the next-generation RTD structures and integration method, detailed studies were performed on the tradeoffs among the various process steps. Minimum alignment tolerances dictate the size and length of the interconnects and integration pads, and parastic capacitance was analyzed as a function of controllable process parameters and the layout

design rules that these process options dictate. The most optimistic results indicate a total interconnect capacitance of 10 fF, on the order of the minimum-geometry RTD device capacitance, and a typical gate capacitance for 0.5 μm CMOS circuits.

- These limitations indicate that thin-film integrated RTD-CMOS hybrid circuits would be best used for the high-power, high-speed circuitry, but they would not be as well suited to high-density, low-power digital logic and memory relative to the best CMOS equivalents in silicon. Because the thin-film integration method developed is adaptable to three-terminal InP-based devices (FETs or HBTs) or optoelectronics such as lasers, it is expected that the same conclusions would apply.

2. TECHNICAL PROGRESS

This chapter summarizes the technical progress under the program. We present accomplishments in sequence, starting from design, then proceeding to circuit layout, fabrication, and test results.

2.1 Progress in Circuit Design

2.1.1 MOSIS Chip Submissions

Four sets of experimental chips were fabricated by MOSIS for use in CMOS/RTD integration. The first two chips were fabricated using a conservative MOSIS 0.8 μm process to provide static protection for the probing pads, and the latter two submissions used a 0.5 μm process. These submissions are referred to as, respectively, MOSIS-3, MOSIS-4, MOSIS-5, and QMOS-1.

The RTD integration area for MOSIS-3 was approximately 800 × 800 μm in the center of each chip. However, for MOSIS-4, MOSIS-5, and QMOS-1, the RTD integration area was split up and moved closer to the actual circuitry to reduce interconnect parasitics.

2.1.1.1 MOSIS-3

Figure 2.1-1 shows the MOSIS-3 layout. The overall chip dimensions were 1.96 × 1.96 mm, the minimum limit for MOSIS. The layout scheme included the following three features:

1. Static protection for probing pads to avoid damage to circuitry
2. Independent ground and power supply for each circuit
3. Pads arranged so they surrounded the CMOS circuitry on all four sides. The 40 μm pads on the interior are the RTD interconnect vias. This layout allowed the circuits to be wire-bonded or probed individually.
4. The all-CMOS circuits were placed at the corners of the chip to provide vias to the RTD integration area in the center.

There were four types of circuits on the chip:

1. Multistate SRAM—n-cascode current sourced multipeak RTD SRAM using a single nMOSFET for high input voltage
2. High-Speed Discrete Structures—Drain-loaded and gate-loaded RTD structures with coplanar waveguide probing pads
3. Current-Mode Pulse Amplifier—A self-resetting scheme using two RTDs and a rising edge detector
4. RTD Comparator—A comparator using a clocked reset.

The comparator and the logic circuits were the most complex of these designs. They implemented important functions or served as building blocks for future designs.

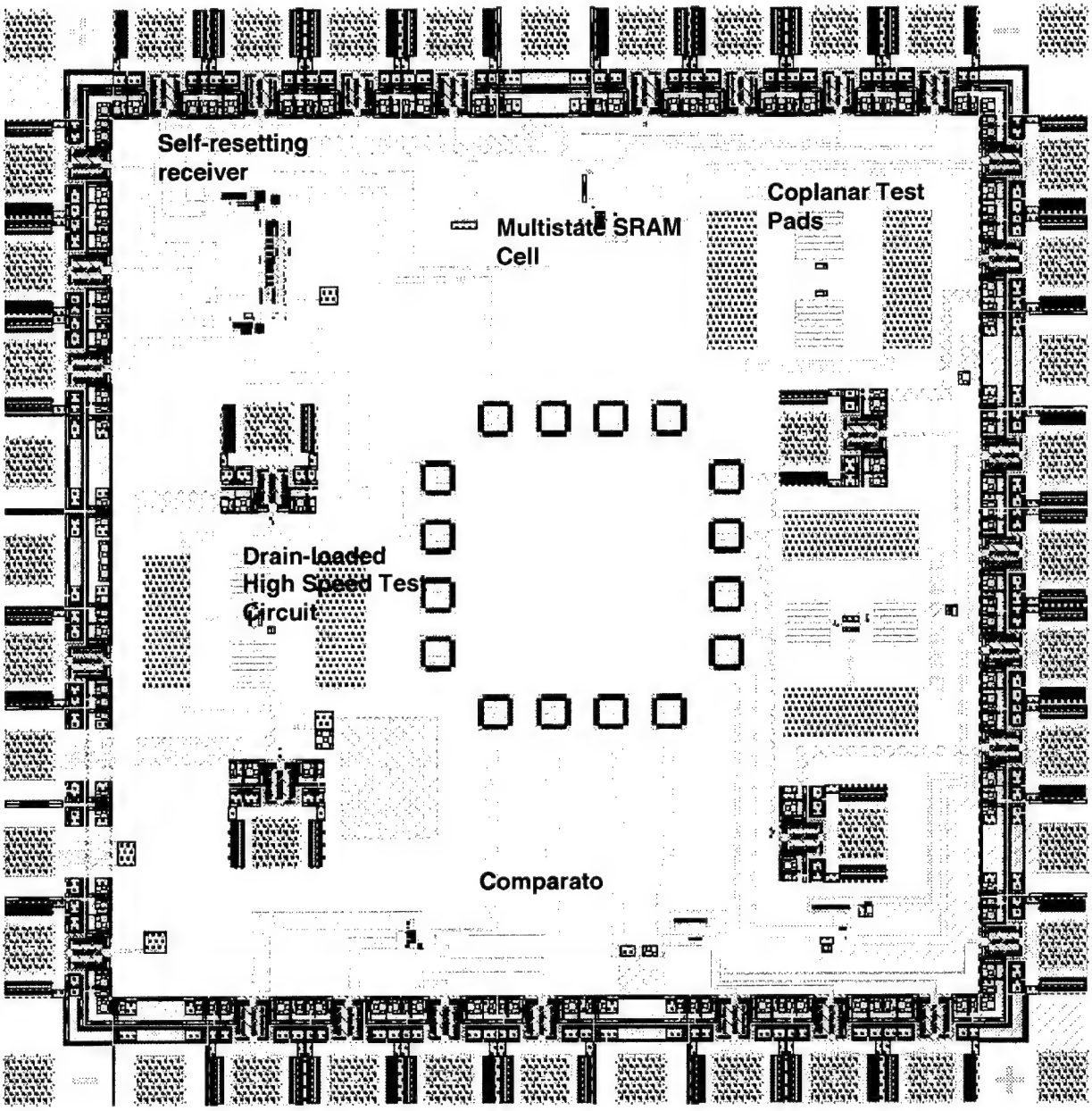


Figure 2.1-1. Layout of the MOSIS-3 chip.

2.1.1.2 MOSIS-4

The pad layout for MOSIS-4 is shown in Figure 2.1-2. The overall chip dimensions were 1.995 × 1.995 mm. The purpose of this chip submission was to enhance the output driving performance of the existing circuitry. After we measured low-drive capability in the output stage of circuitry on the previous chip submission, pad drivers were added to drive the highly capacitive pads.

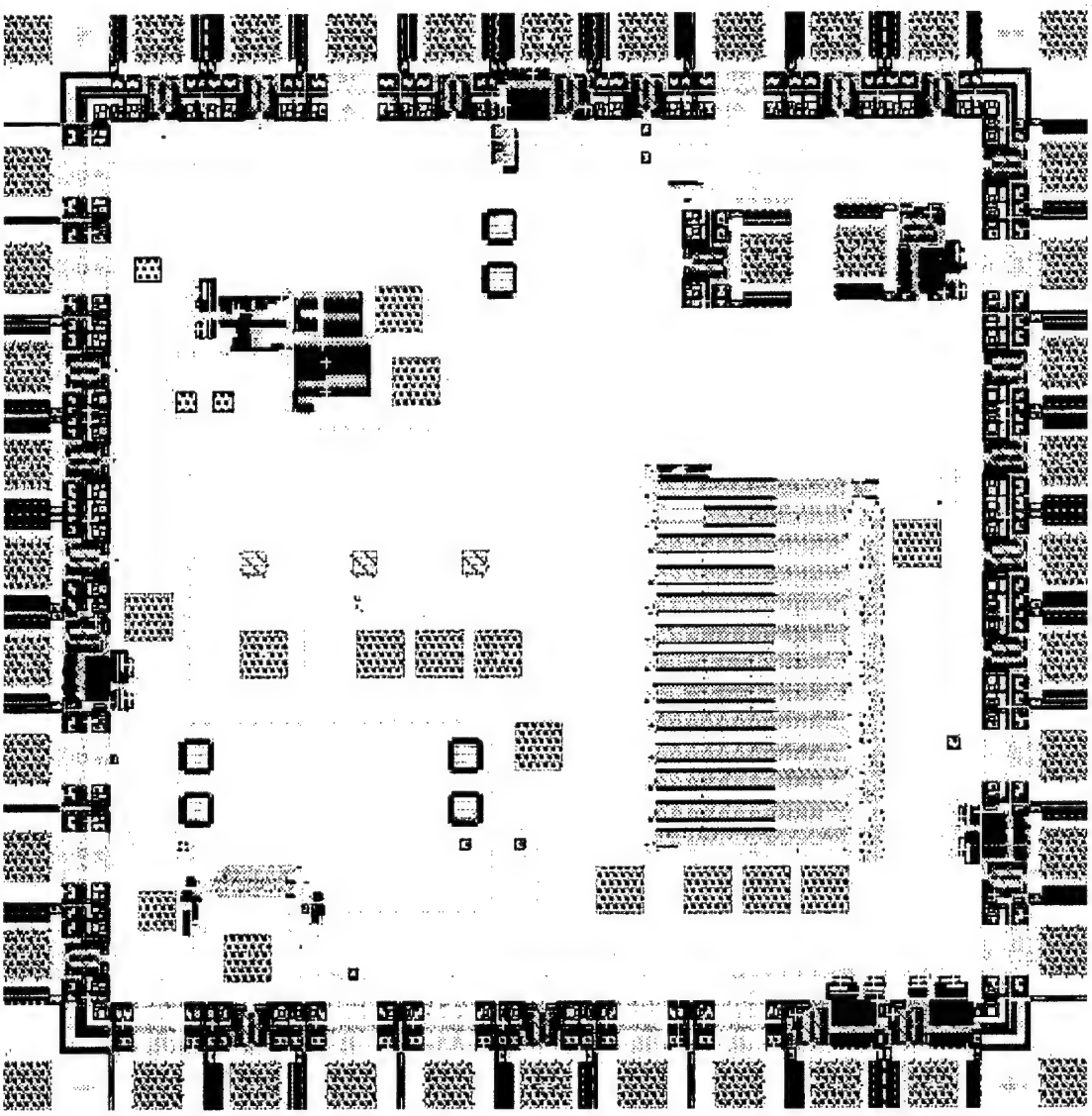


Figure 2.1-2. Layout of the MOSIS-4 chip.

2.1.1.3 MOSIS-5

The pad layout for MOSIS-5 is shown in Figure 2.1-3. The overall chip dimensions were 1.995 × 1.995 mm. MOSIS-5 contained the same circuits as MOSIS-4. The circuit designs and layout were optimized for high speed and low power, assuming very low parasitics associated with integration of the RTDs. Robustness and tunability were sacrificed to achieve the highest possible performance.

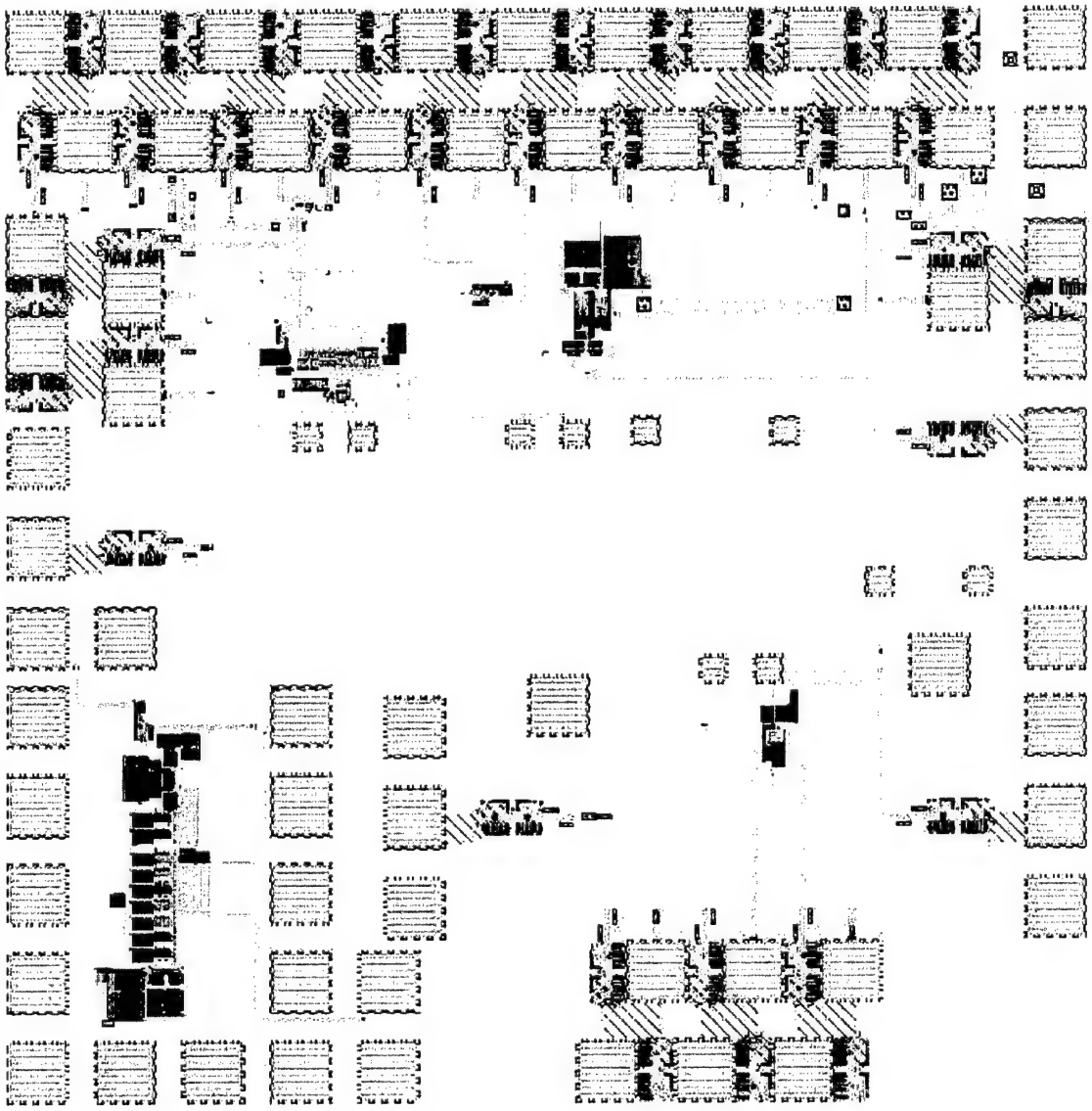


Figure 2.1-3. Layout of the MOSIS-5 chip.

2.1.1.4 QMOS-1

The layout for QMOS-1 is shown in Figure 2.1-4. The overall chip dimensions are 2.5×2.5 mm. The extra area outside the perimeter (300 μm in each direction) eases the processing of chips of these dimensions.

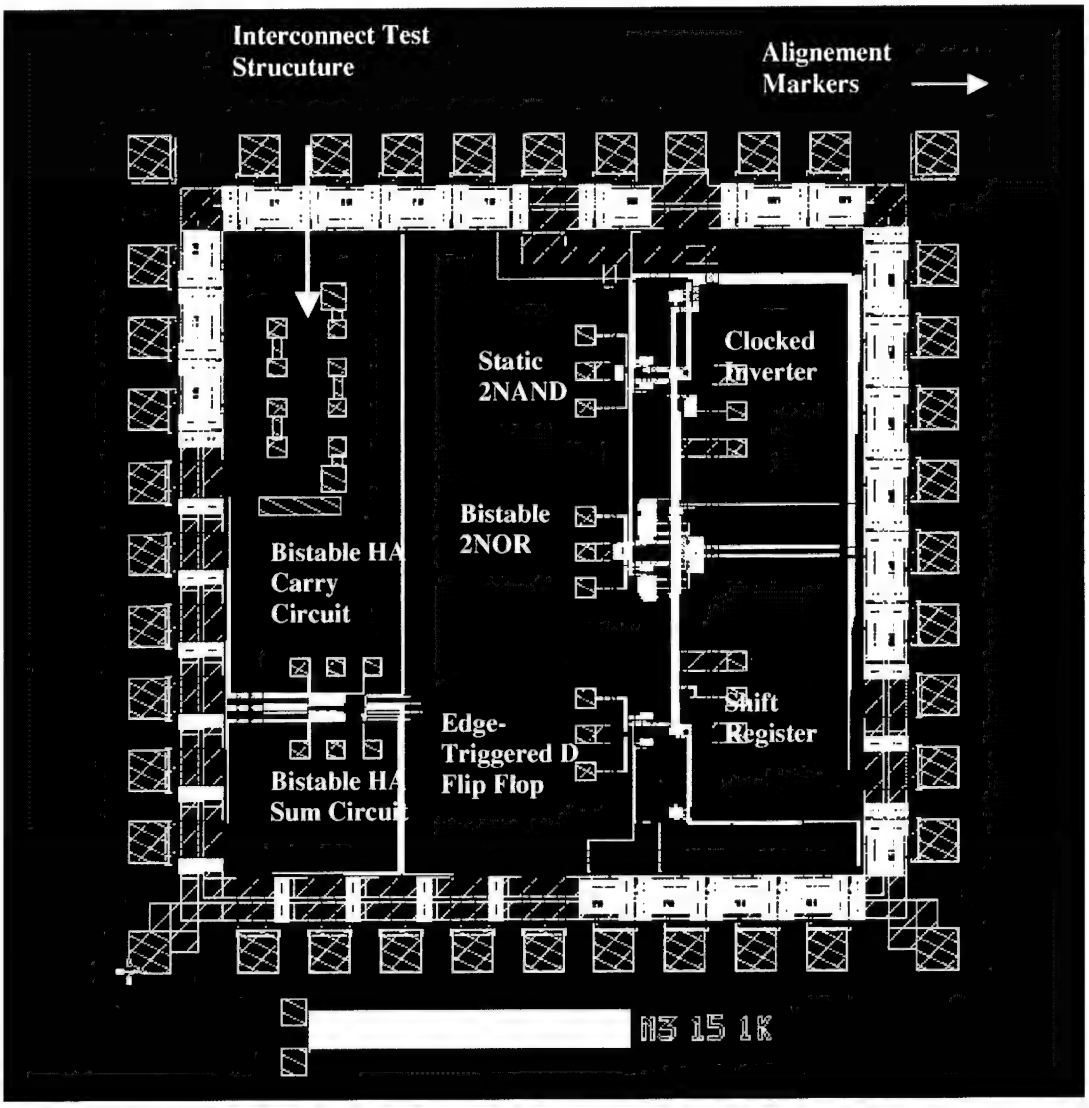


Figure 2.1-4. Layout of the QMOS-1 chip (2.5 × 2.5 μm) in 0.5 μm CMOS.

The following table summarizes the circuits shown in the QMOS-1 chip:

Circuit		# MOSFETs	# RTDs
2-Input Static NAND		2	1
Clocked Inverter		3	2
2-Input Bistable NOR		4	1
Shift Register		6	2
Edge-Triggered D Flip-Flop		6	2
Bistable Half Adder	Carry	4	1
	Sum	6	1

2.2 RTD/CMOS Comparator

Figure 2.2-1 shows a schematic for the RTD/CMOS current mode comparator developed in the program. A reset clock was used to select the lower stable state during a transition of input current from high to low. The output switches to a high voltage state when the input current reaches the peak current of RTD. In this circuit, two current mirrors were used to support peak current (I_P) and input current (I_{in}). A reset signal was used to hold the voltage across RTD less than its peak current voltage (V_P) before the decision point.

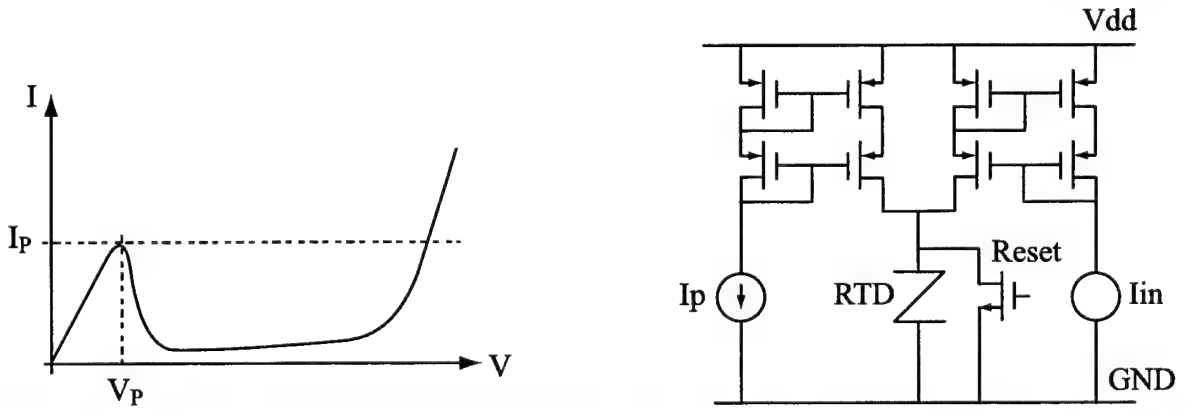


Figure 2.2-1. Schematic of the RTD/CMOS comparator, with the RTD I-V characteristic used in simulation.

Simulation of the designed comparator assuming minimal RTD and integration parasitics is provided below. A sample simulation plot is shown in Figure 2.2-2.

79 μA Peak Current RTD

- Maximum Frequency : 200 MHz
- Power Consumption : 240 μμW

400 μA Peak Current RTD

- Maximum Frequency : 800 MHz
- Power Consumption : 2.4 mW

The layout of this RTD/CMOS comparator for MOSIS-3 submission in the 0.8 μm CMOS process is shown in Figure 2.2-3.

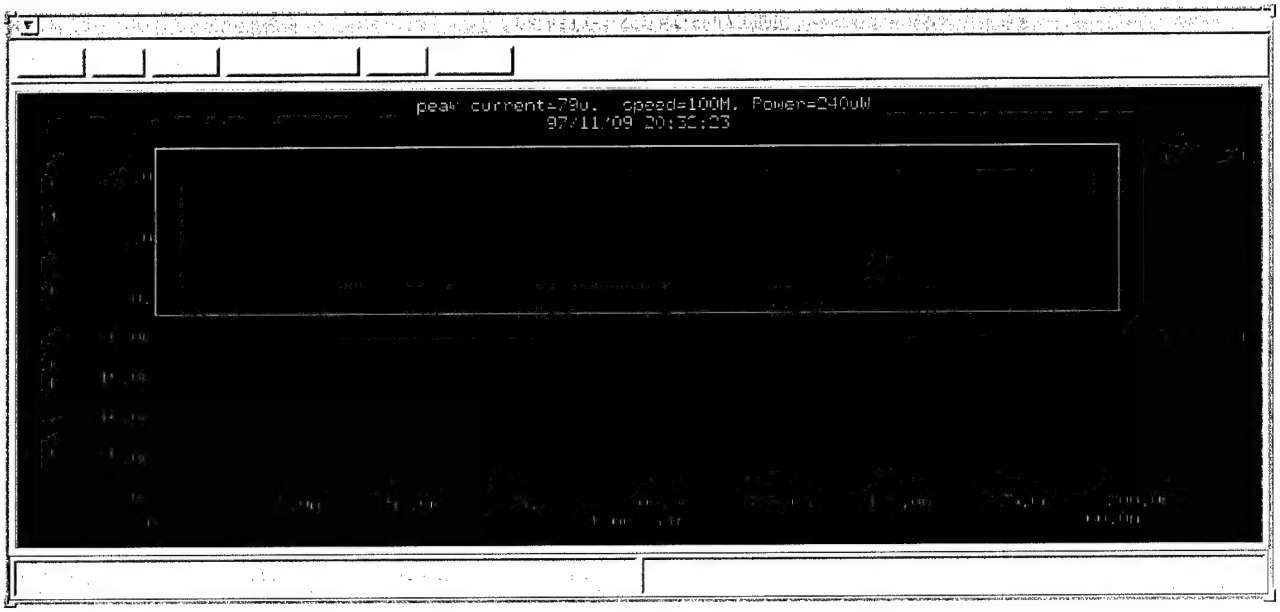


Figure 2.2-2. Simulation sample of RTD/CMOS comparator.

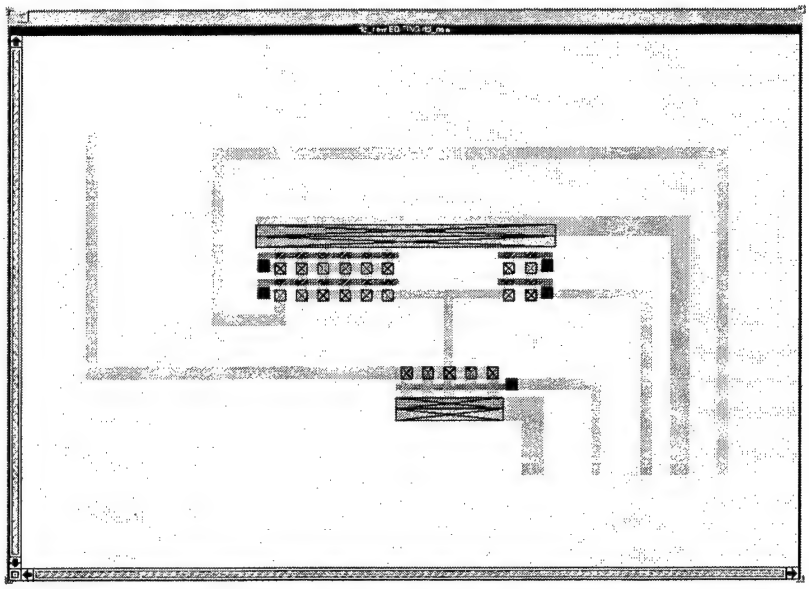


Figure 2.2-3. Layout of the RTD/CMOS comparator.

The comparator circuit also was submitted for MOSIS-4 with drivers added to enable high-speed testing of this circuit after RTD integration. The driver circuits are fully explained in Section 2.4. Also, to provide a higher speed demonstration, the comparator was resubmitted for MOSIS-5 in a more aggressive 0.5 μm process.

2.3 Current-Mode Pulse Amplifier

This amplifier circuit (Figure 2.3-1) employs a self-resetting architecture. By using two RTDs, this circuit avoids the need for an external reset signal. This circuit is a modified version of the MOSIS-2 design and incorporates the use of rising edge detectors to allow for self-resetting operation of the RTDs. This circuitry uses three different bias lines, two for RTDs and one for the rising edge detector circuit. The amplifier operates in current mode and needs two bias currents for the two RTDs. While the amplifier submitted in the previous MOSIS runs required RTDs with higher peak currents, this design submitted in MOSIS-3 can be used with RTDs that have very low peak current. By using an RTD with peak current of 4 μA, the power consumption of this circuit reduces to 40 μW. This design also provides a very high transimpedance gain of hundreds of megohms.

This pulse amplifier was submitted again in MOSIS-4 with slight modifications and a different transistor size. While both MOSIS-3 and MOSIS-4 circuits were fabricated in 0.8 μm technology, the circuit was also modified and submitted for MOSIS-5 in a 0.5 μm CMOS process.

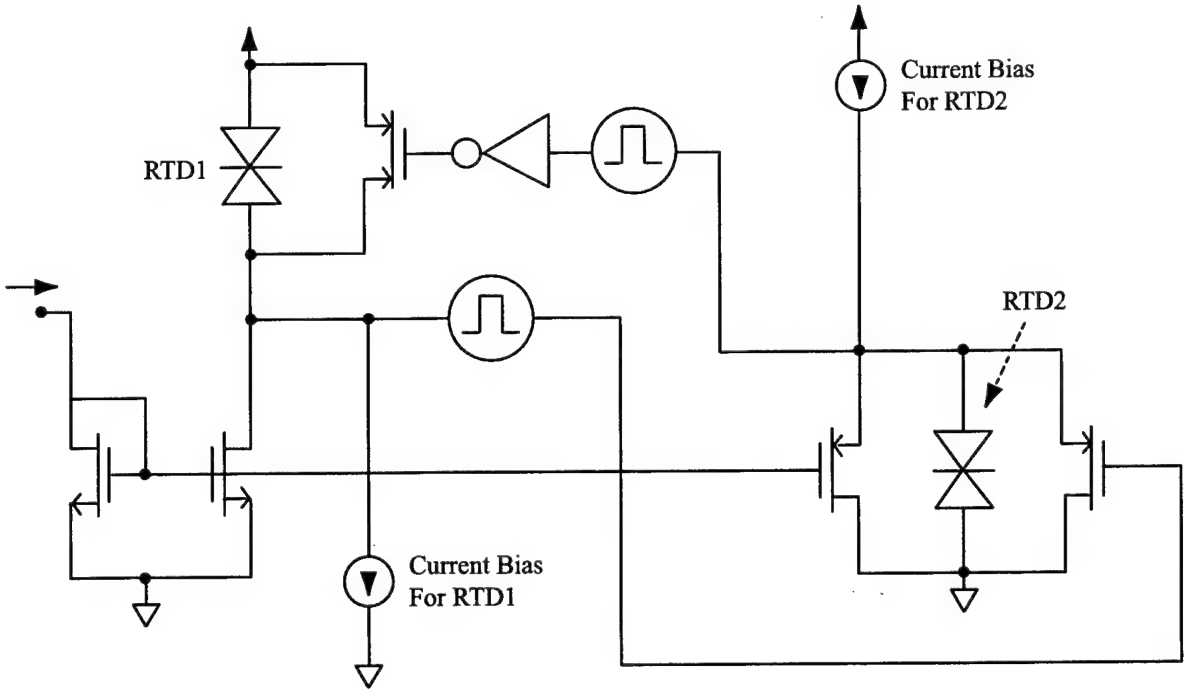
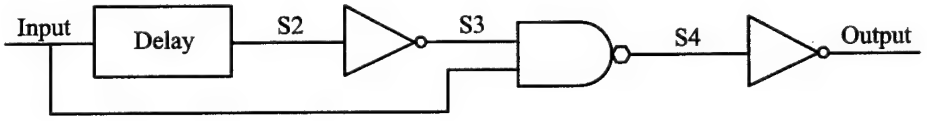


Figure 2.3-1. Schematic of the RTD/CMOS current mode pulse amplifier.



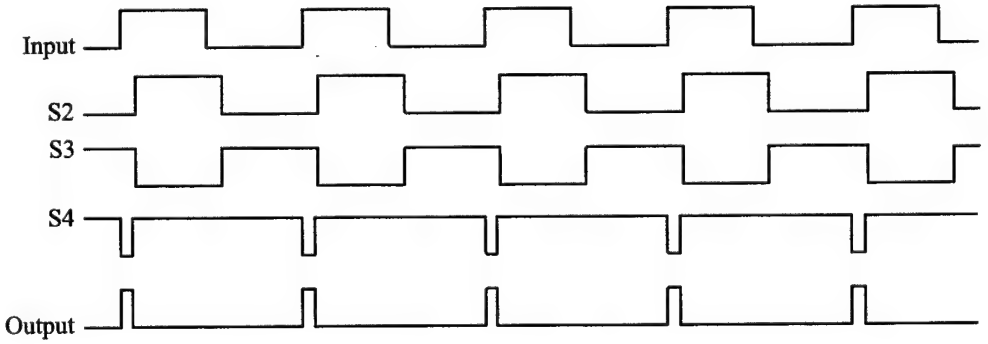


Figure 2.3-2. Block diagram of pulse amplifier rising edge detector.

A sample of the simulation results of the RTD/CMOS pulse amplifier using 40 μA peak current RTDs is shown in Figure 2.3-3. The mask layout for this circuit is shown in Figure 2.3-4.

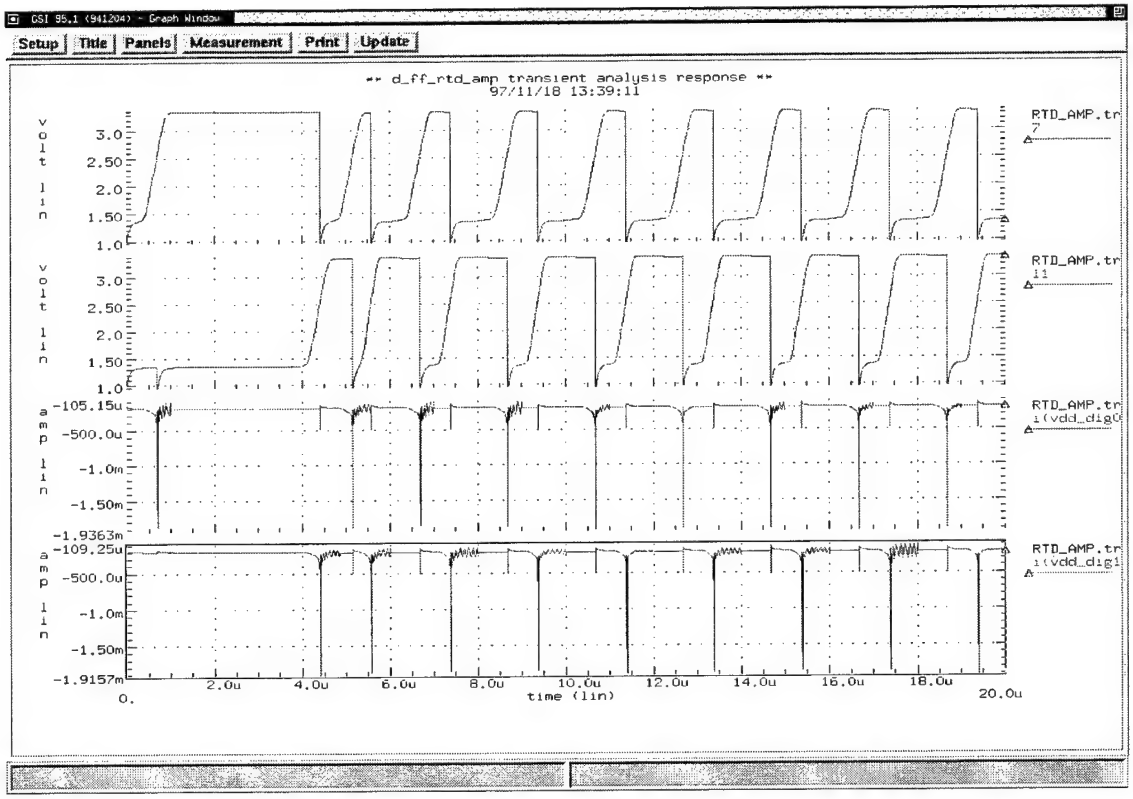


Figure 2.3-3. Simulation sample of the RTD/CMOS pulse amplifier.

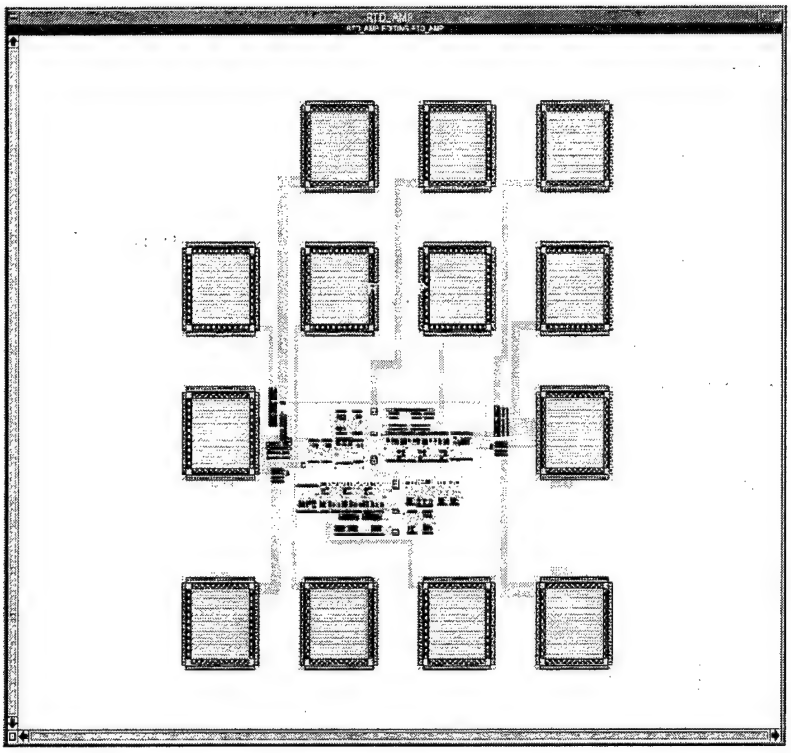


Figure 2.3-4. Layout of the RTD/CMOS pulse amplifier.

2.4 Pad Driver

Two designs were developed for the pad driver circuits. Each configuration has its own characteristics as described next.

Modification of MOSIS Digital Pad

A MOSIS digital pad was fabricated and tested successfully up to a reasonable speed range (≈100 Mbps). However, since we could not be sure about the transition voltage of the RTD circuit output due to CMOS process variations, additional circuitry was required in front of the digital pad to allow adjustment of the transition voltage for the MOSIS digital pad driver (Figure 2.4-1).

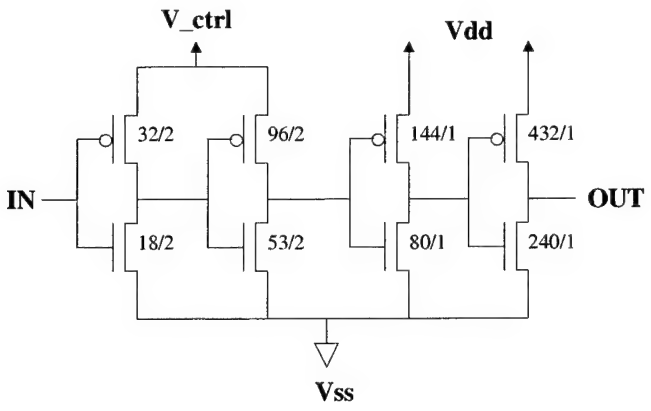


Figure 2.4-1. Modified MOSIS pad driver.

Differential Pad Driver

The MOSIS pad driver had a simple and single-ended configuration that made its design relatively straight forward. However, when simulated under realistic load conditions, it showed an unstable oscillation due to interconnect inductance effects.

For this reason, we developed a differential circuit configuration to stabilize the current into the circuit and to reduce transmission line effects. In this design, the speed and the amount of current to drive the output stage was made adjustable by controlling the bias current injected into the circuit. An adjustable digital input stage also was employed, just as in the modified MOSIS pad driver design. This is shown in Figure 2.4-2.

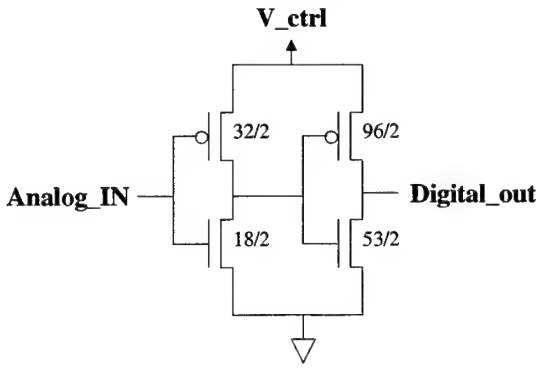


Figure 2.4-2. Adjustable transition input stage.

The purpose of first stage is to limit the maximum digital signal swing to a standard level suitable for driving the next following output pad driving stage. In this first stage, the swing range was designed to be controllable by adjusting the current bias (Figure 2.4-3).

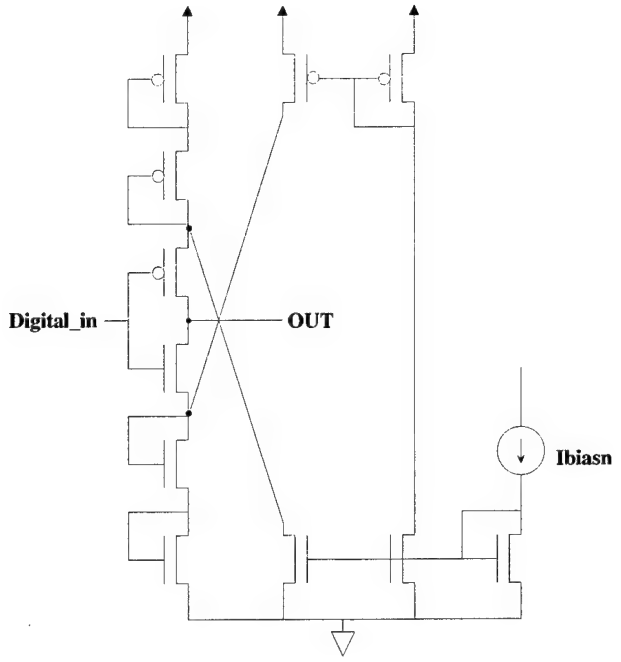


Figure 2.4-3. Digital input-converting stage.

The output pad driving stage shown in Figure 2.4-4 was designed to generate ECL-compatible output signals using two inverted analog inputs from the previous stage.

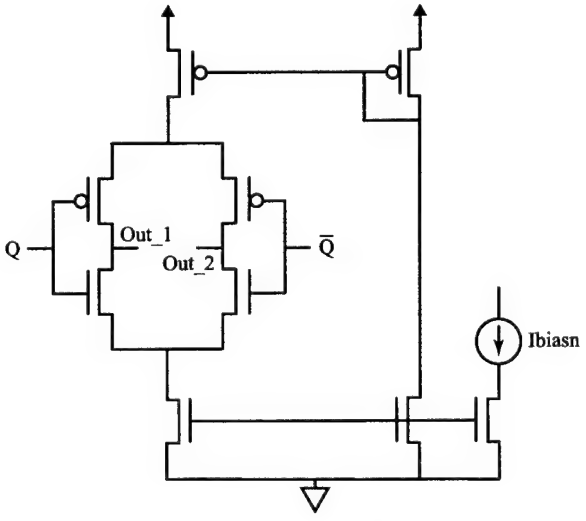


Figure 2.4-4. Output pad driving stage.

2.5 High-Speed Discrete Structures

Both drain-loaded and gate-loaded high-speed RTD configurations were included in the MOSIS submissions. Integration and characterization of these fundamental circuits yielded valuable data on their use as building blocks in future designs. Shorted and opened pad structures were included in MOSIS-3 and loaded structures were added on MOSIS-4 to de-embed the pad parasitics. Standard 150 μm pitch coplanar probe pads were incorporated in the layout of these structures. Figures 2.5-1 and 2.5-2 show the schematic and layout of the two structures, and Figure 2.5-3 shows the layout of the open structure used for de-embedding the pad parasitics.

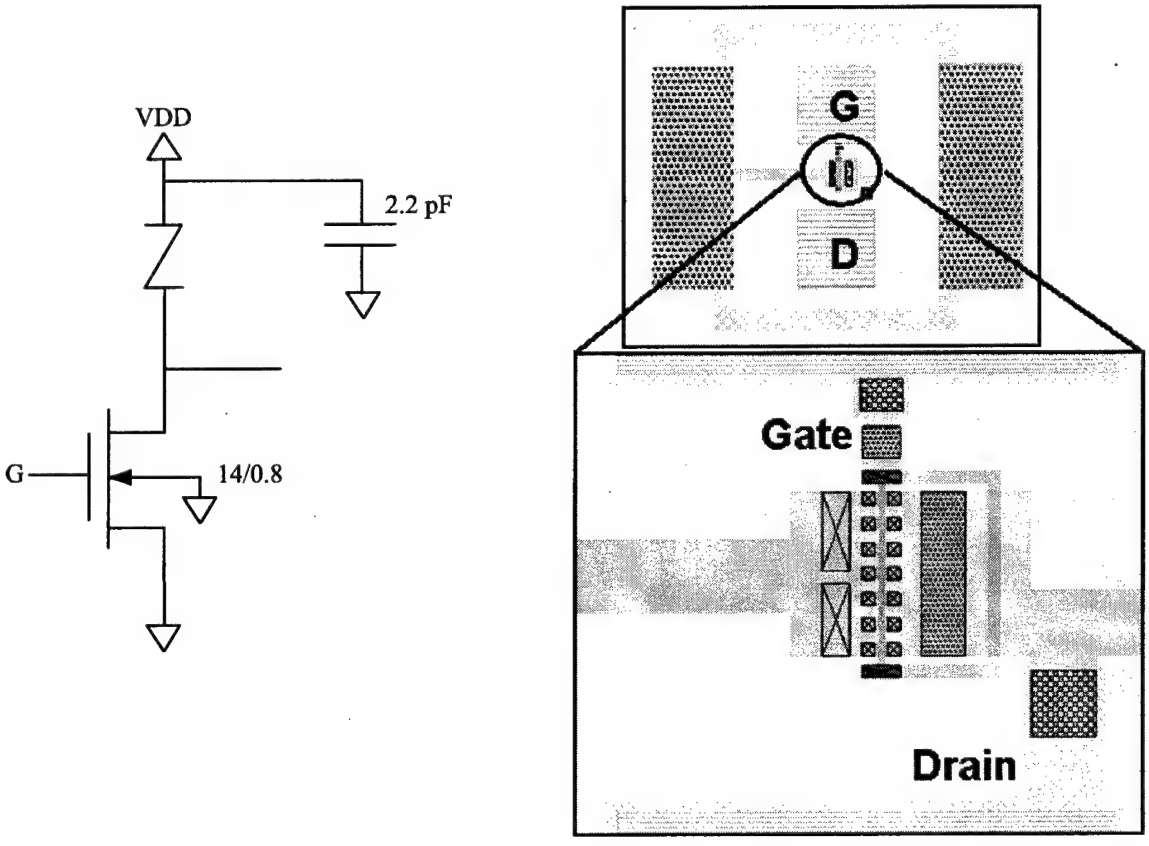


Figure 2.5-1. Schematic and layout of a drain-loaded structure.

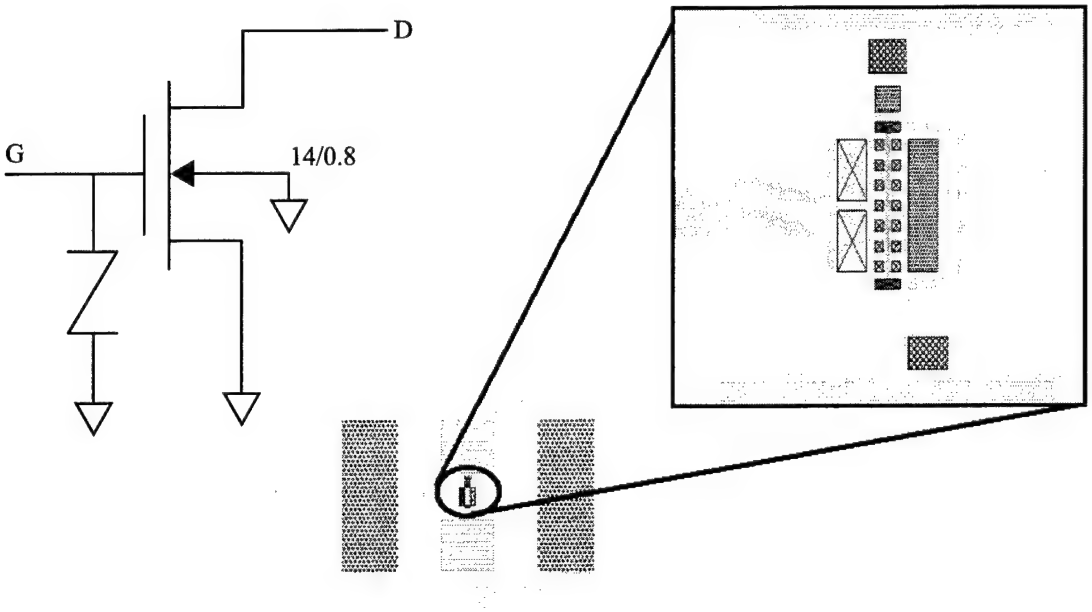


Figure 2.5-2. Schematic and layout of a gate-loaded structure.

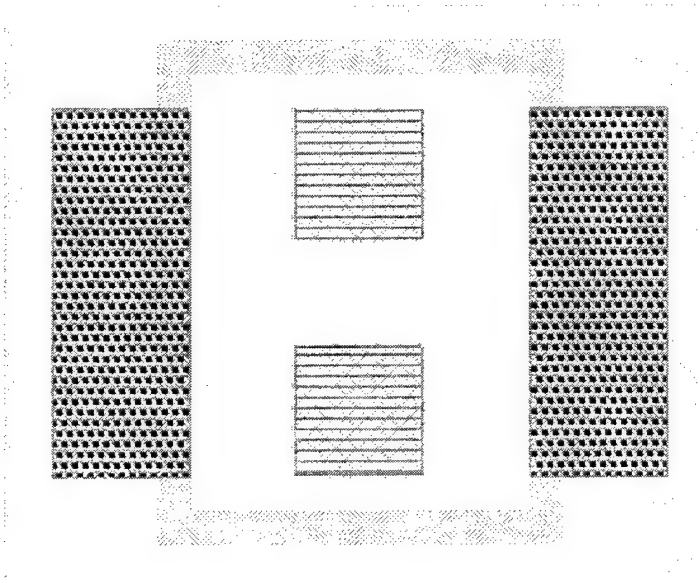


Figure 2.5-3. Layout of an RF 150 μm coplanar open structure.

2.6 Multistate SRAM Cell

Figure 2.6-1 shows the circuit schematic for the developed multistate SRAM cell using a multipeak RTD (MPRTD). A similar circuit with slight modifications from MOSIS-2 was submitted in MOSIS-3 0.8 μm process with static protection and higher current. The RTD has three peaks, resulting in a four-state SRAM. The cell is a simple n-cascode with an MPRTD load. Figure 2.6-2 shows the SRAM layout. The cascode transfer curve and MPRTD load line are shown in Figure 2.6-3. A transient simulation of the circuit is also included, with $V_{dd} = 3.3$ V.

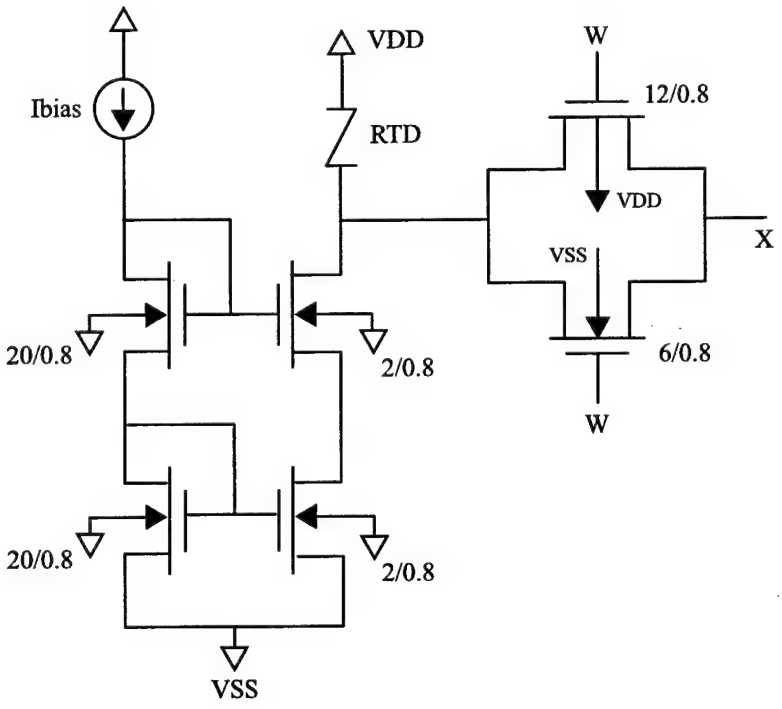


Figure 2.6-1. Schematic of multistate SRAM circuit.

The double cascode current mirror was chosen to give a higher output resistance as compared to a single transistor. The current mirror supplied a maximum of about 100 μA with 3.3 V at the DC input. In practice, the current mirror should not source more than about 50 μA because higher static currents degrade transistor performance and can cause premature failure. The transmission gate is used at input/output point because a single nFET cannot transmit higher voltages without a significant voltage drop.

The MPRTD transfer curve used is shown in Figure 2.6-3. The peak voltage separation was chosen to be about 0.9 V to allow for greater noise margins and voltage drops through the transmission gate. High peak-to-valley ratios are preferred. Finally, all valley currents in the I-V curve should be as closely matched as possible. In particular, the last (highest voltage) valley current tended to be higher than the others, especially after substrate removal. Low current in the RTD is preferable because it decreases power consumption and improves the transmission gate performance, although write speed may also be decreased.

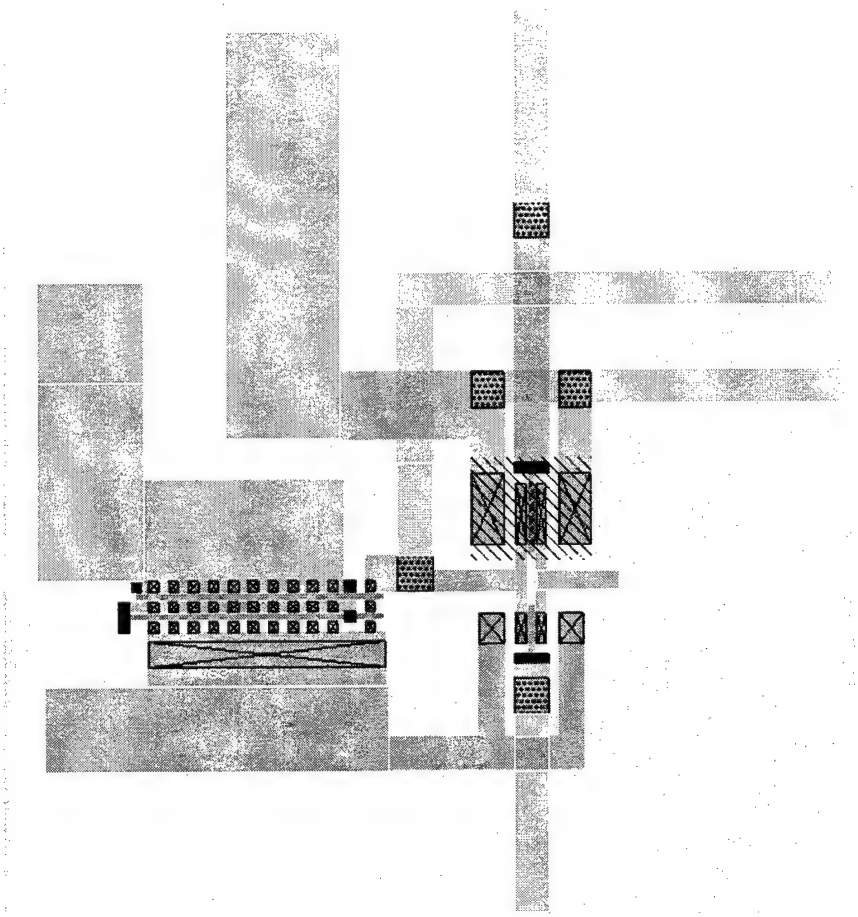


Figure 2.6-2. Multistate SRAM layout.

The input transistors in the double cascode current mirror were oversized so that the DC bias current could be fixed at approximately 500 μA. This allowed for greater relative stability in the overall bias current. The transistors in the transmission gate also were enlarged to reduce the voltage drop from the RTD to the output node during reading or writing. The layout configuration allowed the RTD storage node to be probed directly to facilitate testing and better observe the memory cell's switching characteristics.

This multistate SRAM, shown with a three-peak RTD, has four states. The stable operating points are indicated by the intersection of the n-cascode transfer curve (broken line in Figure 2.6-3) with the positive differential resistance regions of the RTD load line (solid line).

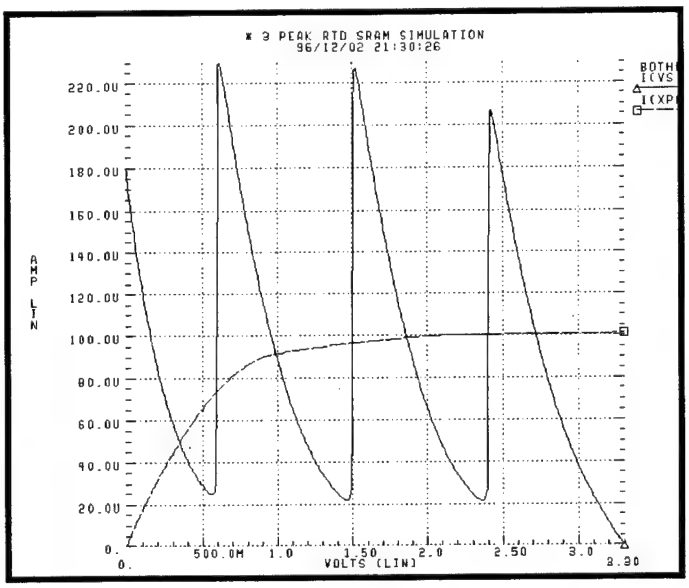


Figure 2.6-3. DC operation of the multistate SRAM.

In the transient simulation shown in Figure 2.6-4, the word line levels are indicated by the dash-dot line. The word level is 3.3 V, higher than the highest voltage level. The input voltage is indicated by the solid line, stepping through the four logic levels. The broken line indicates the voltage at the RTD storage node, which stabilizes at the proper static operating point once the write is complete.

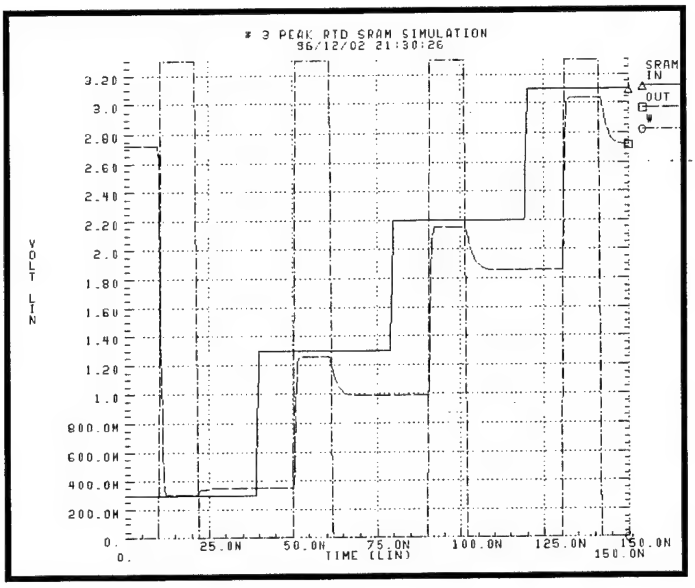


Figure 2.6-4. Transient operation of the multistate SRAM.

2.7 Two RTD SRAM Cell

We developed a dual-RTD static memory cell that employed a latched RTD pair to convert a conventional one-transistor dynamic memory cell into a static memory cell. This design is novel in that it operated much like a dynamic RAM, while not requiring the normal periodic state refresh cycle. The concept of the RTD binary TSRAM cell is illustrated in Figure 2.7-1. The storage capacitor is replaced by the intrinsic device capacitance of the RTD pair, which acts as a charge-keeper that eliminates the need for refresh cycles. The RTD currents can be very low (pA) since they need only compensate for the leakage and subthreshold current within the transistor.

Figure 2.7-1. Evolution of the RTD/MOS TSRAM (b) from the conventional one-transistor MOS DRAM (a).

The silicon-based TSRAM is useful where there the leakage currents are higher than a normal DRAM transistor. This may occur when large, dense on-chip memory is needed in a conventional digital CMOS process. Since refresh rates are proportional to the worst-case transistor leakage current, a dramatic improvement in standby power can be realized with the TSRAM, when compared to conventional SRAM and DRAM technologies.

2.8. QMOS Digital Logic Designs

2.8.1. Static QMOS Circuits

A static QMOS gate may consist of an RTD pullup load and a pulldown network of n-transistors that determines the logic operation performed by the gate. A generic static QMOS logic gate is illustrated in Figure 2.8-1a). Figure 2.8-2(b) shows the load lines of this static QMOS logic gate. The principle of operation of a static QMOS gate is as follows.

When the inputs, I_1, I_2, . . ., I_m, of the static QMOS gate are such that the pulldown network is turned off, there is no current flow through the circuit and, hence, the voltage at node out equals the supply voltage (i.e., logic high).

The transistors in the pulldown network are so designed that when the inputs I_1, I_2, . . ., I_m, of the static QMOS gate are such that the pulldown network is turned on, the current through the circuit exceeds the peak current of the RTD. This causes the RTD operating point to jump to PDR2, resulting in the output voltage at node out going low, corresponding to a logic low.

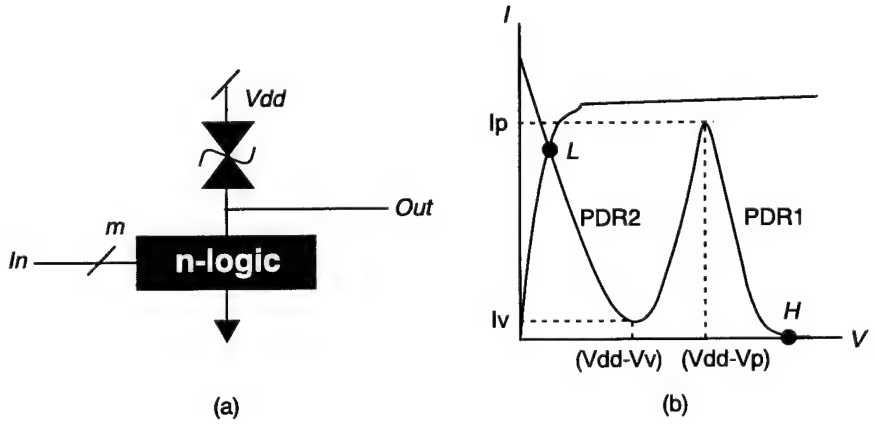


Figure 2.8-1. (a) Static RTD-MOSFET logic gate and (b) load lines for static RTD-MOSFET gate operating point.

2.8.2. Bistable QMOS Circuits

A binary logic circuit is said to operate in bistable mode when its output is latched, and any change in the input is reflected in the output only when a clock or other evaluation signal is applied. The bistable mode has been used in several earlier technologies, notably in superconducting logic. Superconducting logic typically uses a multiphase AC power source to periodically reset and evaluate each gate. Similar logic using resonant tunneling devices has been proposed by several authors. The chief disadvantage of these circuits is the requirement of an AC power source whose frequency determines the maximum switching frequency. The RTD-MOS logic circuits described below use a DC power supply and multiphase clocks, but the clock signals are not required to supply large amounts of power as in the case of the earlier circuits. The operating principle of the new bistable element may be understood by considering the simplified circuit shown in Figure 2.8-2 (a). The RTD forms the active load in the circuit. There are m inputs in the n-logic block that determines the circuit function, one clock transistor that controls the evaluation of the gate, and a bias transistor that maintains quiescent current through the RTD while also controlling the precharging of the gate output. Figure 2.8-2 (b) shows the load lines for the bistable logic gate. Switching of the bias transistor is used to reset the state of the gate or to maintain a quiescent current through the RTD that is between its peak and valley currents. The clock transistor is designed so that if the n-block is turned on, turning the clock transistor on will cause the current through the RTD to exceed its peak current value, and thus switching the state of the gate.

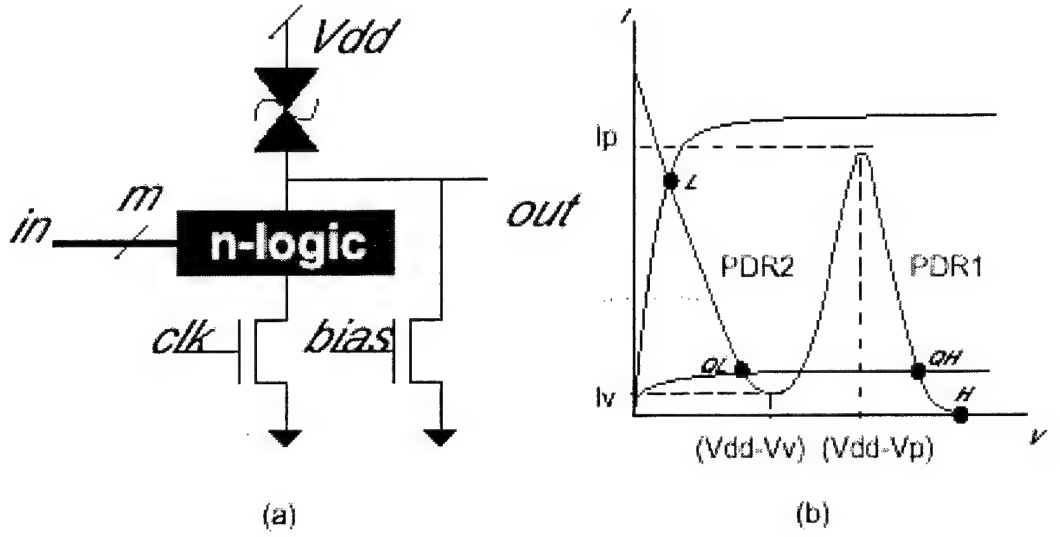


Figure 2.8-2. (a) Bistable-mode RTD-MOSFET logic gate and (b) load lines for RTD-MOSFET gate operating point.

The sequential operation of the gate is enumerated below.

Inputs I_1 through I_m change. The clk signal is held low, thus preventing evaluation of the output node by the n-logic block.

The bias signal goes low, forcing the current through the RTD to zero. When the current falls below the valley current, I_v, of the RTD, the out node is pulled high. This is point H, as indicated in Figure 2.8-2 (b).

The bias signal is then set to logic high. The out node remains high. The current through the RTD is now the quiescent current, I_q, and the circuit operating point changes to QH in the load lines of Figure 2.8-2 (b).

The clk signal goes high. If the inputs I_1 through I_m are such that the n-logic block is turned on, then turning the clock transistor on causes the current through the RTD to exceed the peak current, I_p, of the RTD. This causes a jump to the second positive differential resistance (PDR2) region of the RTD characteristic corresponding to V_RTD > V_v, where V_RTD is the voltage across the RTD and V_v is the valley voltage of the RTD. This results in

the out node going low. The circuit is at operating point L. If the n-logic block is not turned on, the RTD current does not increase beyond I_q and the circuit operating point remains at QH in the first positive differential resistance region (PDR1) of the RTD, where V_RTD < V_p (with V_p being the RTD peak voltage). Thus, out remains high.

The clk signal goes low so that no current flows through the n-logic block. The output voltage at node out reaches a stable value corresponding to whether the RTD was in PDR1 (operating point QH) or PDR2 (operating point QL) in the previous step of the sequence.

2.8.3. QMOS Edge-Triggered Flip-Flop Circuits

RTD-based circuits have unique self-latching properties, as discussed in the previous subsection. It is well known that edge-triggering is commonly required in VLSI circuits for accurate samplingof an input at clock edge so that further circuits are immune to variations in the input signal (which might otherwise lead to false evaluation). We designed a family of edge-triggered flip-flops using RTDs and MOSFETs. Figure 2.8-3 is a block diagram of a QMOS positive edge-triggered D flip-flop circuit.

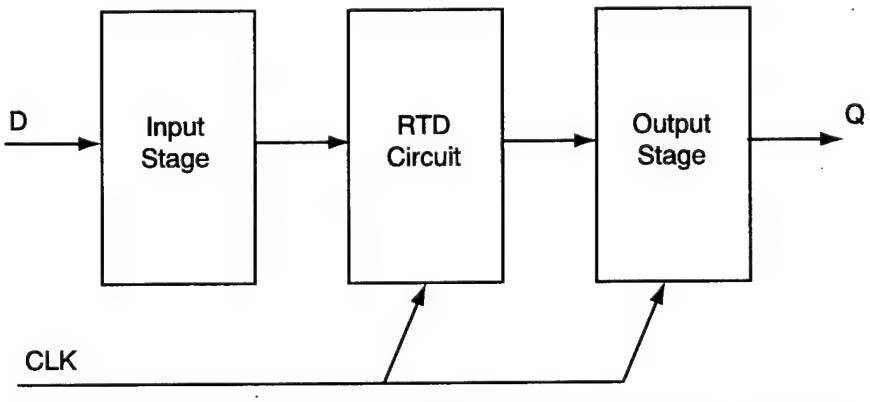


Figure 2.8-3. Block diagram of a QMOS positive edge-triggered D flip-flop.

A Monte-Carlo simulation of the QMOS D flip-flop and a conventional true single-phase clock (TSPC) CMOS flip-flop using the same MOS devices are shown in Figure 2.8-4. It can be seen that the QMOS flip-flop operates at a higher frequency than the TSPC flip-flop.

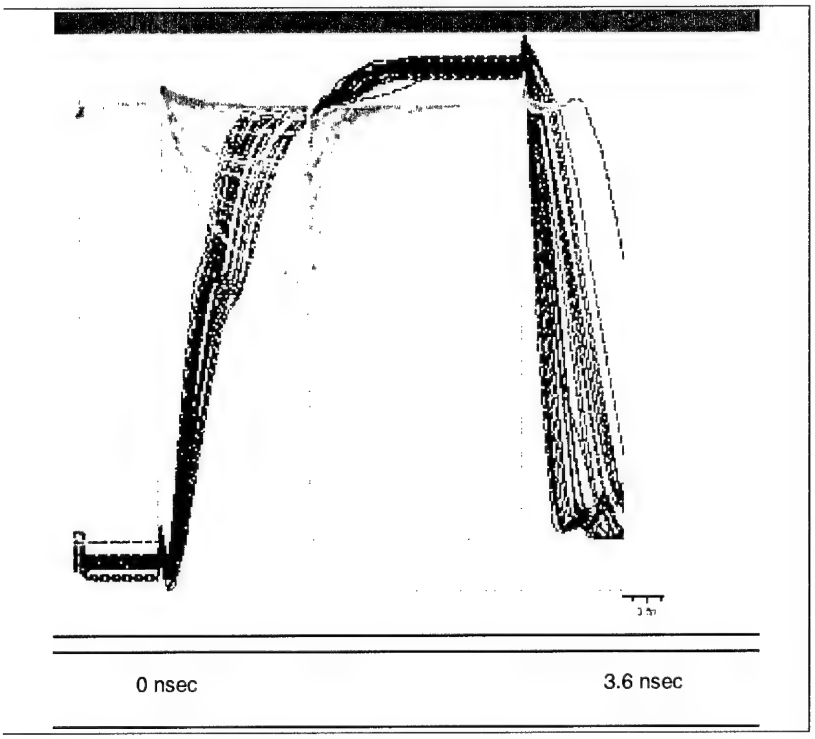


Figure 2.8-4. Simulation traces for a QMOS D flip-flop.

2.8.4. QMOS Bistable Full Adder

Figure 2.8-5 shows the schematic of the full adder circuit. The majority function that gives the carry output is evaluated on Phase 1 of the clock. Each clock phase consists of a pulse on the bias line followed by an evaluation clock pulse in accordance with the operation sequence of the gate explained in Section 2. Bistable buffers clocked on Phase 1 are required to synchronize inputs to the sum stage of the circuit, which is evaluated on Phase 2 of the clock. Simulation traces of the 1-bit full adder circuit using nMOS pull-down logic are shown in Figure 2.8-6.

We designed a majority carry circuit based on a 2-phase clock. A majority logic function can provide the carry output term in a full-adder. Each clock phase consists of a pulse

on the bias line followed by an evaluation clock pulse in accordance with the operation sequence of the gate. Bistable buffers clocked on Phase 1 synchronize inputs to the sum stage of the circuit which is evaluated on Phase 2 of the clock

In this circuit, two computations can be active concurrently and this form of nanopipelining improves the throughput of the system. The RTD-MOSFET bistable full adder uses 5 RTDs and 20 n-MOSFETs. To convert a standard 24-MOSFET static CMOS adder to a similar gate-level pipelined adder, we would require an additional 40 transistors for 5 latches required for the carry, the sum and the three input signals. The addition of these latches to a conventional CMOS circuit would provide the pipelining advantage but would increase the stage delay and area due to the additional latches. Thus, the RTD-MOSFET logic family has advantage over conventional CMOS logic in terms of greater circuit compactness and improved speed.

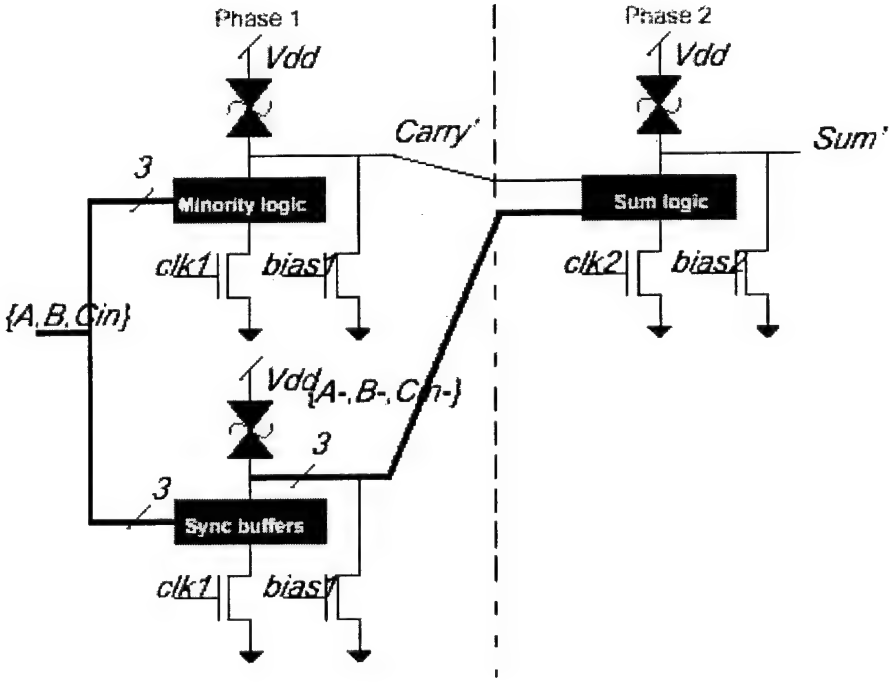


Figure 2.8-5. Pipelined RTD-MOSFET full adder schematic.

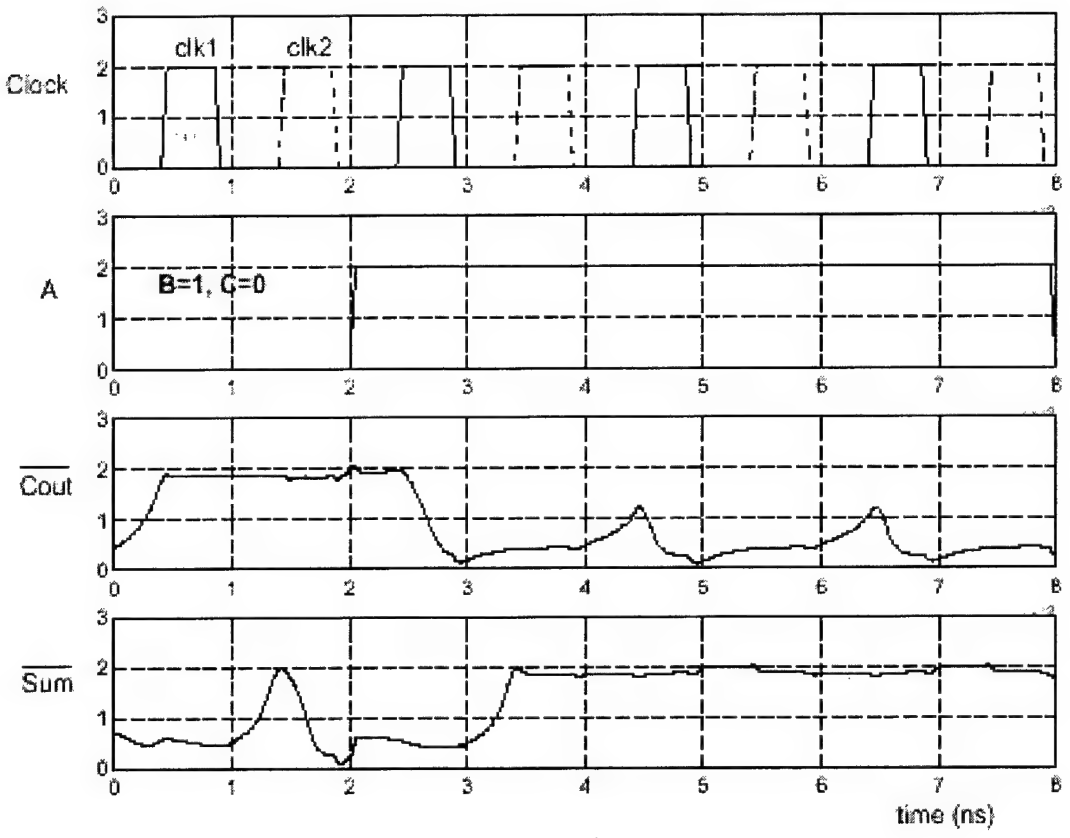


Figure 2.8-6. Pipelined RTD-MOSFET full adder simulation.

3. PROGRESS IN PROCESS DEVELOPMENT

3.1 RTD Characteristics

The resonant tunneling diodes used for the integration process were fabricated on an InP substrate. The layer structure is shown below in Figure 3.1-1. The structure employs strain-compensated AlAs and InAs layers in the barrier and well region of the device to allow for a wide range of peak currents and peak voltages to match the circuit requirements. A plot of the peak currents as a function of the InAlAs pre-barrier thickness is shown in Figure 3.1-2. The only intentional variation within one set of devices was a change in pre-barrier thickness. The two sets represent two different quantum well thicknesses. The available peak current densities span four orders of magnitude and follow an exponential dependence on the pre-barrier thickness as expected.

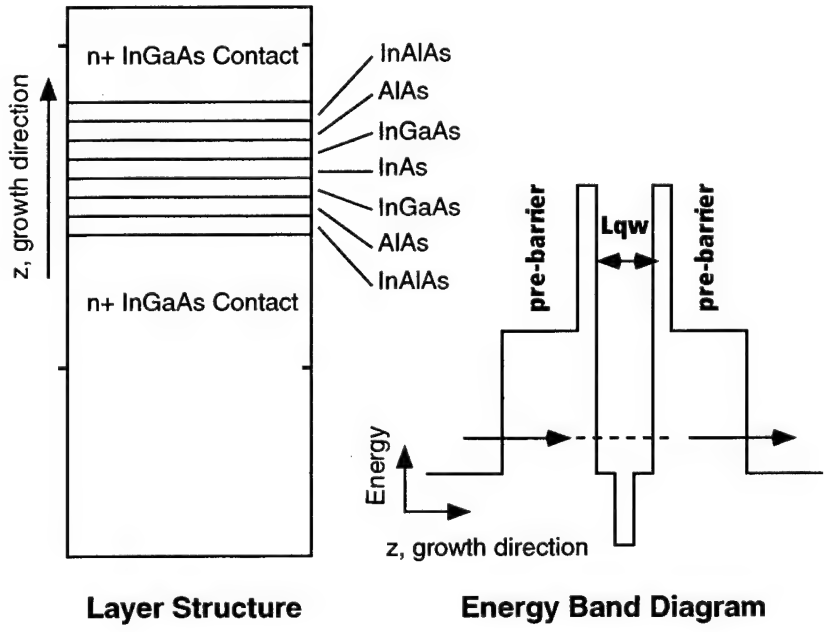


Figure 3.1-1. RTD layer diagram and energy band diagram. The arrows in the energy band diagram show the resonant tunneling through the quasi-bound state in the RTD quantum well.

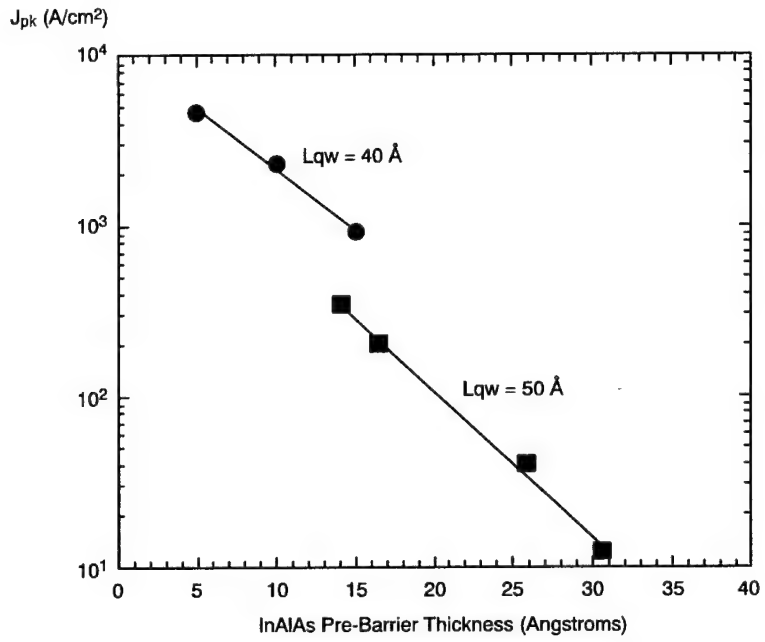


Figure 3.1-2. RTD peak current density as a function of InAlAs pre-barrier thickness.

3.2 Thin-film Transfer of InP-Based Devices

In the InP system, the selective etching of the InP growth substrate can be accomplished using an HCl or HCl:H_3PO_4 (3:1) solution to separate the thin-film epitaxial devices from the substrate. Since there is a high degree of selectivity between InP and InGaAs for these etch solutions, no sacrificial etch stop layer is necessary, and InGaAs can be used as the etch stop layer. Devices were grown and fabricated at Raytheon, and transferred to Georgia Tech for the substrate removal and CMOS integration.

RTD Arrays: Substrate Removal and Bonding with Backside Metallization

To investigate the capacity to integrate arrays of RTDs to silicon, arrays of RTDs were transferred to silicon substrates. The epitaxial structure was grown using molecular beam epitaxy, while the arrays of RTD mesas were defined with electron beam lithography with sizes ranging from 0.2×0.2 μm to 1.0×1.0 μm. Our (Raytheon's) FOX passivation process is employed instead of the 500 – 1000 Å Si_3N_4 that is typically used in the devices used for substrate removal and transfer. In addition to studying the potential of integrating arrays, this investigation demonstrated the feasibility of using this FOX passivation and planarization

process for future thin-film structures. The FOX process would be desirable due to its greatly reduced parasitic capacitance and degree of planarization relative to thin Si_3N_4 used previously. The set of RTDs in the array are electrically linked with a Ti/Au contact over the FOX. For each device size, five different array sizes were incorporated onto the InP wafer: 1, 10, 100, 1000, and 10,000 RTDs. A photomicrograph of the chip is shown in Figure 3.2-1. The epitaxial structure shown of the devices are shown in Figure 3.2-2.

Figure 3.2-3 illustrates the basic steps for substrate removal and bonding to a host substrate. A handling layer (Apiezon W wax) was used to preserve the integrity and relative spatial orientation of the thin-film devices. This Apiezon W handling layer was applied before the substrate removal, and also serves to protect the devices from the wet chemical etching used for the InP substrate removal. After the substrate is removed, the devices and handling layer are briefly immersed in a weak oxide etch ($NH_4OH:H_2O$ 1:15), then rinsed in deionized water. Because these RTD arrays require backside contacting, a Ti/Au contact was evaporated onto the back of the thin-film devices, contacting the n^+ InGaAs layer closest to the InP substrate. The devices were subsequently transferred and metal-metal bonded to a Ti/Au-plated silicon host substrate. The handling layer was dissolved in TCE. A final rapid thermal anneal bonds the metal layers to provide good adhesion and electrical contact.

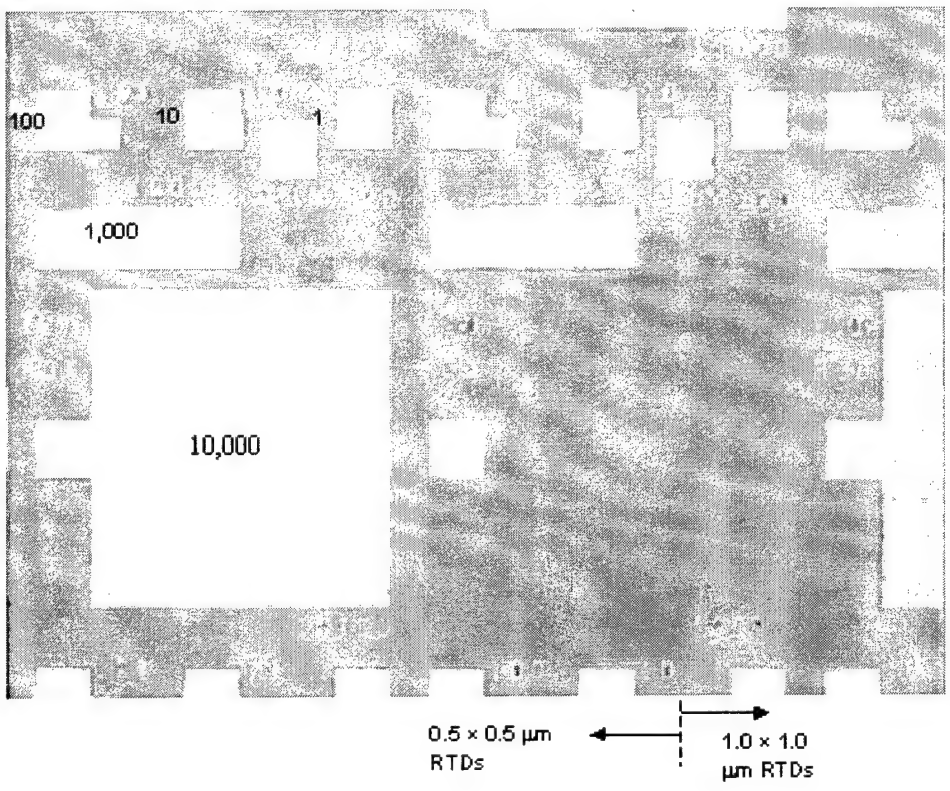


Figure 3.2-1. RTD arrays on die. Only the 0.5 μm and the 1.0 μm devices are illustrated. For all the device sizes, there are arrays of 1, 10, 100, 1000, and 10,000 RTDs.

n^+ InGaAs	600 Å	1e19 Si
n InGaAs	200 Å	1e18 Si
i InGaAs	50 Å	
i AlAs	20 Å	
i InGaAs	6 Å	
i InAs	18 Å	
i InGaAs	6 Å	
i AlAs	20 Å	
i InAlAs	21 Å	
i AlAs	20 Å	
i InGaAs	6 Å	
i InAs	18 Å	
i InGaAs	6 Å	
i AlAs	20 Å	
i InGaAs	50 Å	
n InGaAs	200 Å	1e18 Si
n^+ InGaAs	2000 Å	1e19 Si
InP Substrate		

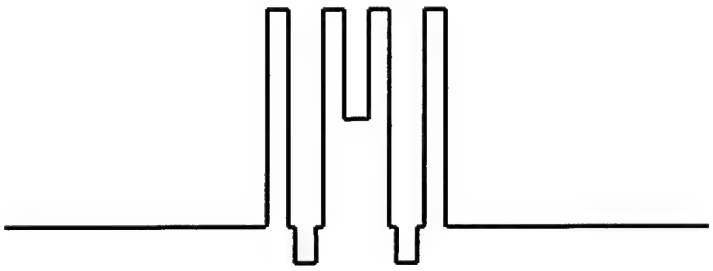


Figure 3.2-2. The epitaxial structure and conduction band profile of the devices used in the integration of RTD arrays.

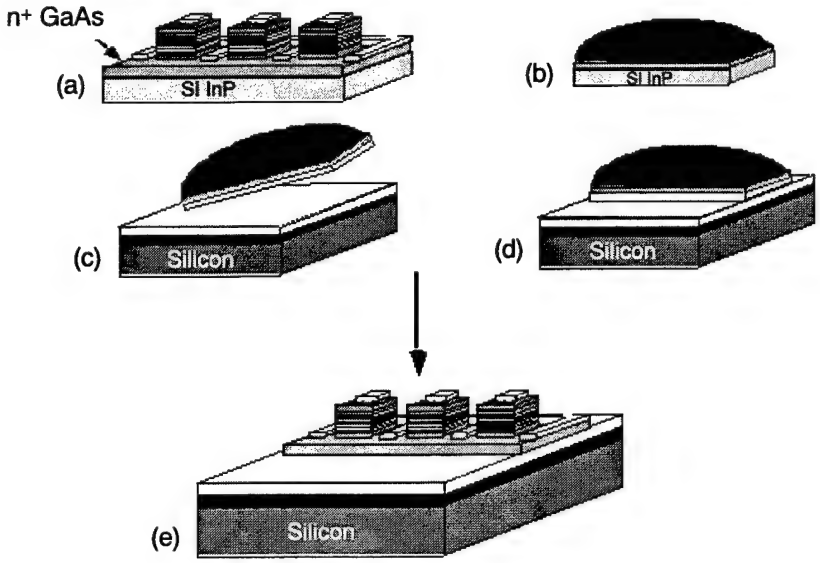


Figure 3.2-3. Substrate removal and bonding of RTDs onto silicon host substrates. The on-wafer devices (a) are covered with the Apiezon W handling layer (b). The substrate is removed, and the thin-film structure is metallized with Ti/Au for the back contact (c). The devices are transferred and bonded to gold-plated silicon (d). Removal of the Apiezon W handling layer and annealing of the metal-to-metal bond completes the process (e).

Epitaxial Liftoff of HBTs

Epitaxial liftoff of HBTs grown on InP was performed similarly to the older process used for RTD transfer that we described in Figure 3.2-3. Back metallization was omitted because there is no need for a back contact. HBTs are first coated with a carrier Apiezon W handling layer, then the InP substrate is removed by an HCl or HCl:H_3PO_4 (3:1 or 4:1) solution. The n-InGaAs subcollector layer that exists between the InP substrate and the actual devices acts as a stop-etch layer to shield the devices from damage. The devices are then bonded to a quartz, polished sapphire, or beryllia substrate by van der Waals forces. The handling layer is then removed and the devices are characterized. Figure 3.2-4 shows a coupled HBT.

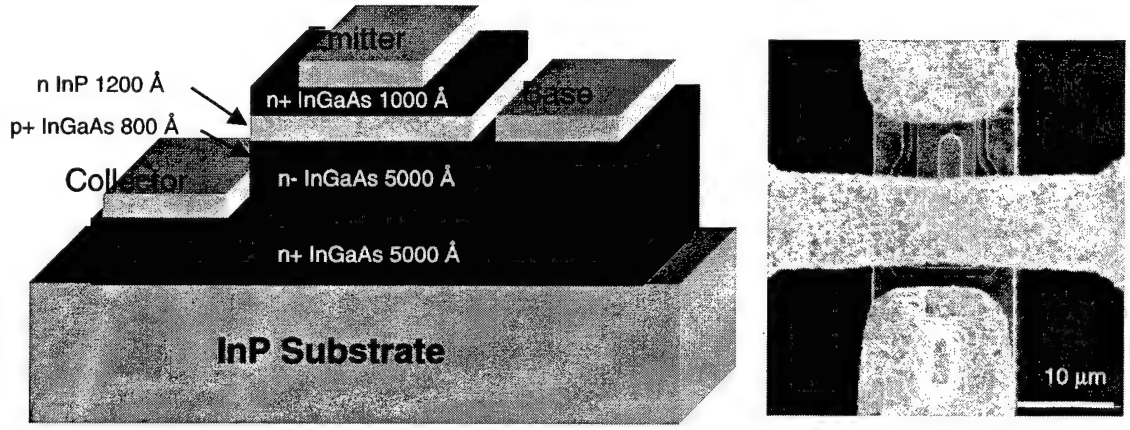


Figure 3.2-4. The epitaxial structure of the InP-based HBT.

3.3 Integration of Devices onto Circuits

The techniques illustrated in Figure 3.2-3 do not allow the thin-film devices to be aligned precisely with respect to features on the host substrate. This causes difficulty in the manufacturable post-bonding metallization that is necessary to contact a device to a circuit on the host silicon substrate. By using a transparent transfer diaphragm in the transfer process, the thin-film devices can be aligned with respect to features on the host substrate, with the versatility to pick and place individual devices, as shown in Figure 3.3-1.

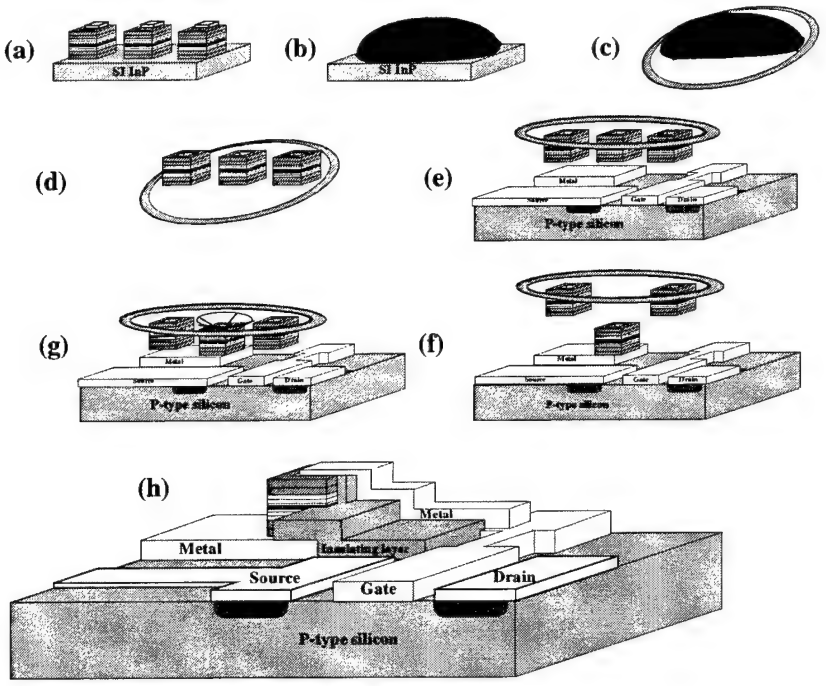


Figure 3.3-1. Substrate Removal and Bonding Using a Transfer Diaphragm. The transfer diaphragm enables the aligning and bonding of the thin-film devices to the host substrate as well as giving the ability to process both the top and bottom of the device. Post-processing of the top contact pads is done after the device has been contact-bonded to the host substrate.

In the alignable thin-film transfer process illustrated in Figure 3.3-1, the device is flipped before transfer. To ensure good contact to the metal pad on the host substrate, the top surface of the thin-film structure to be transferred should be planar. This need for planarity required additional processing of the InP-based devices, in this case RTDs, before substrate removal.

A typical epitaxial layer stack of the RTDs used for integration with CMOS circuits is shown in Figure 3.3-2. The thickness of the InAlAs pre-barriers was selected to give the desired peak current density, 12 A/cm^2, which reflects the need to match the RTD currents to the current drive capability of the CMOS circuitry. The RTD mesas were patterned in sizes ranging from 4×4 μm to 24×24 μm. A thin 500 Å Si_3N_4 layer was deposited for passivation, followed by a via etch to the top of the RTD; 100×100 μm Ti/Au contact pads were evaporated over the nitride to allow for on-wafer testing of the individual devices. A photomicrograph of the initial on-wafer RTDs is shown in Figure 3.3-3 with a profile of the device.

1000 Å $In_{0.35}Ga_{0.74}As$: 5e18 Si
1000 Å $In_{0.35}Ga_{0.74}As$: 1e18 Si
40 Å $In_{0.35}Ga_{0.74}As$
25 Å $In_{0.25}Al_{0.84}As$
25 Å AlAs
15 Å $In_{0.35}Ga_{0.74}As$
25 Å InAs
15 Å $In_{0.35}Ga_{0.74}As$
25 Å AlAs
25 Å $In_{0.25}Al_{0.84}As$
40 Å $In_{0.35}Ga_{0.74}As$
1000 Å $In_{0.35}Ga_{0.74}As$: 1e18 Si
5000 Å $In_{0.35}Ga_{0.74}As$: 5e18 Si
Semi-insulating InP substrate

Figure 3.3-2. A typical epitaxial layer structure of the RTDs used for integration with CMOS circuits.

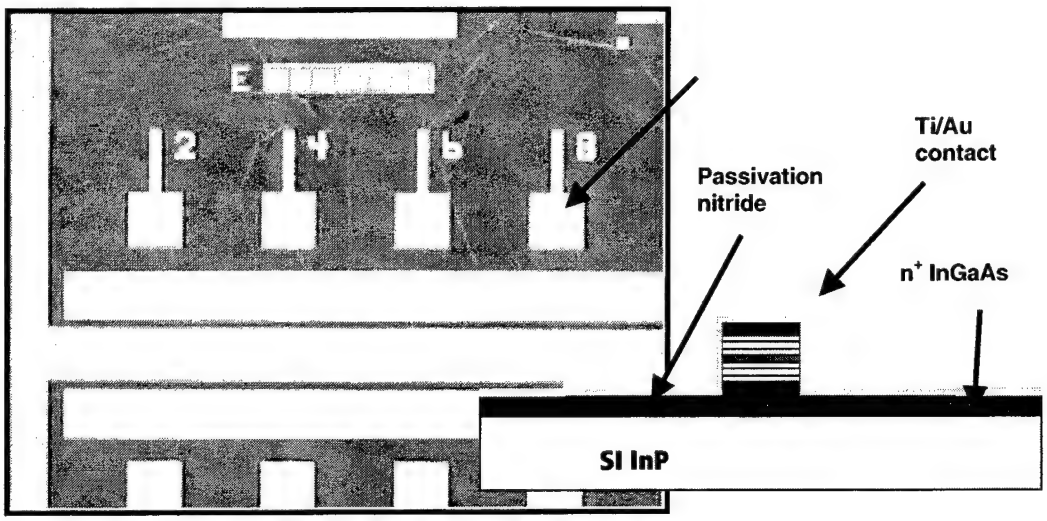


Figure 3.3-3. The on-wafer RTD structures before planarization.

The first step in the planarization of the RTDs was the removal of the large bonding pad with wet chemical etching. A 3 μm polyimide layer was spin-coated and cured. In addition to planarizing the top surface of the thin-film device for good bonding, the polyimide layer reduces the parasitic capacitance between the top contact and the back n-InGaAs layer. A via surrounding the RTD mesa was etched in the polyimide by reactive ion etching (RIE), followed by patterning and metallization of a 95 × 95 μm Ti/Au top contact pad. Subsequently, a self-aligned etch of the field polyimide, Si_3N_4, and bottom n-InGaAs layer isolates each RTD. The final on-wafer structure is shown in Figure 3.3-4 (a), with the individual RTD structures linked only by the InP substrate.

The substrate is then removed with the alignable process detailed in Section 3.2, with no back-metallization after substrate removal. Before transfer to the CMOS chip, a 100 × 100 μm Ti/Pt/Au bonding pad was evaporated onto the CMOS chip, overlapping one of the aluminum pads to the CMOS circuits, as shown in the photograph of Figure 3.3-5 (a). An RTD was then aligned and bonded to this pad on the CMOS chip. Polyimide is spun and cured to serve as an interlayer dielectric for the second contact between the RTD and the CMOS circuit. Vias were etched in the polyimide over the RTD and the second CMOS pad. A Ti/Au top contact pad was sputtered and patterned to connect the RTD to the CMOS pad. Finally, the field polyimide was etched, masked by the top contact, in order to access the circuit pads. The integrated RTD/CMOS circuit is schematically illustrated in Figure 3.3-4 (b).

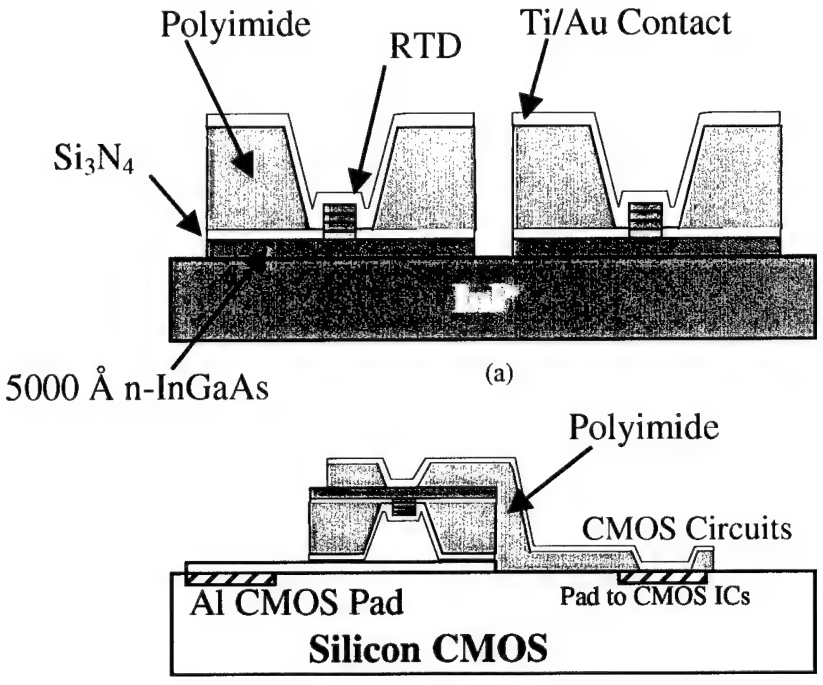


Figure 3.3-4. Thin-film integration of RTDs to CMOS. (a) The planarized RTDs are individually isolated and then separated from the InP substrate, then aligned and bonded to the CMOS chip (b).

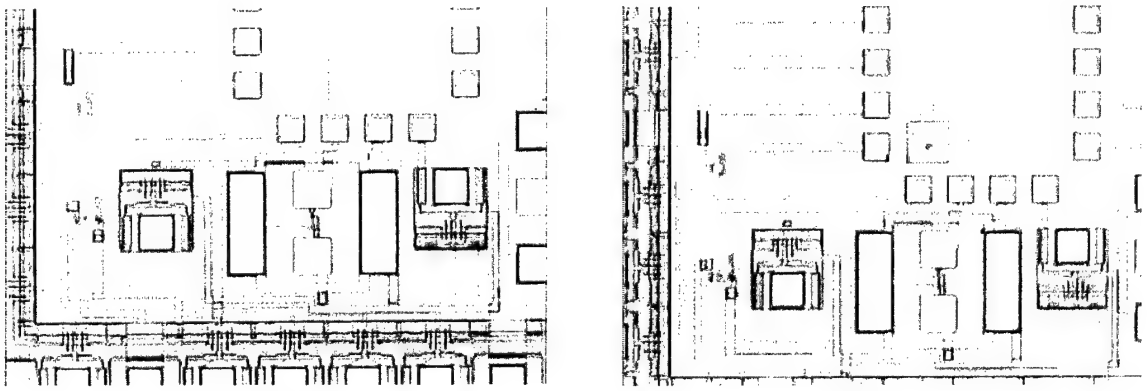


Figure 3.3-5. (a) The CMOS chip with bottom integration pad (100 × 100 μm). (b) The same CMOS chip with the inverted RTD die (95 × 95 μm) transferred and bonded. Post-processing is needed to connect the backside of the RTD to the second CMOS pad.

Figure 3.3-6 shows a completed circuit, using somewhat longer integration interconnects. The use of shortened interconnects, as illustrated in Figure 3.3-5, is one of the process improvements made with successive generations of integrated RTD/CMOS circuits. In addition to the shorter interconnects, the sizes of the transferred RTD die and integration pads have been scaled down substantially, from 200×300 μm die and pad sizes in the early RTD/CMOS circuits to the 95×95 μm dimensions currently used. This is a critical development because pads of this size can approach interconnect parasitic capacitance on the order of 10 fF, where this would be impossible with the larger pads. Finally, the polyimide planarization process improves the yield and reliability of process by allowing for improved bonding and reducing the strain of the transferred thin-film structure. As seen in Figure 3.3-7, there was no degradation in the characteristics of a transferred RTD.

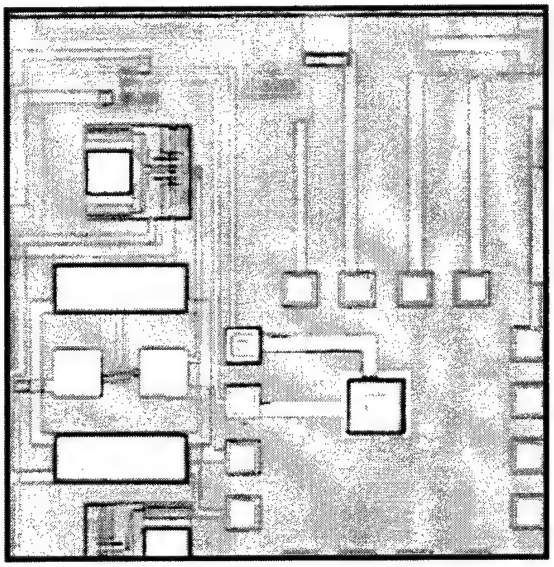


Figure 3.3-6. The completed RTD/CMOS integrated circuit.

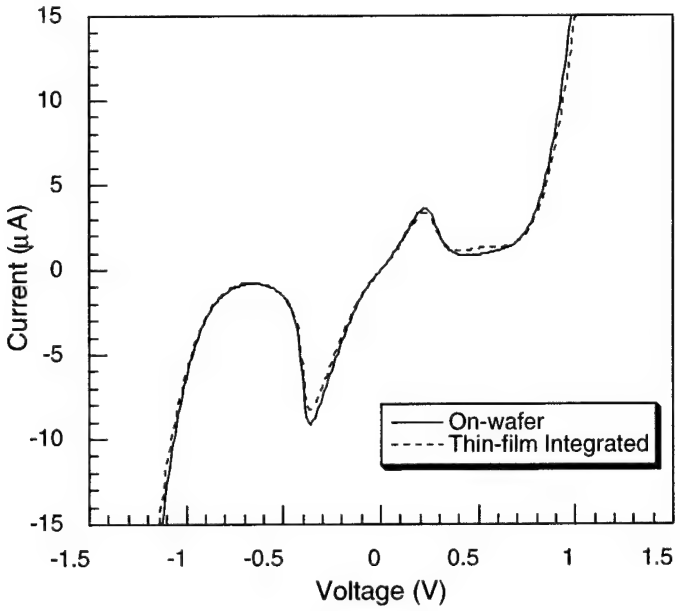


Figure 3.3-7. The current-voltage characteristics of a 6 × 6 μm integrated, low-current-density RTD.

3.4 Process Optimization for Thin-Film Integration

The parasitic capacitance associated with the integration of RTDs to CMOS must be improved to accurately benchmark RTD/CMOS technology in comparison to all-CMOS technology. There is a large parasitic capacitance associated with the thin-film RTD structure shown in Figure 3.3-4 (a) due to the need for the via through the polyimide to overlap the RTD mesa. This results in a high parallel plate capacitance through the 500 Å Si_3N_4 layer. While the bottom integration pad and interconnect have a large parasitic capacitance, it is connected to a power line or the circuit ground in most circuit designs, where the extra capacitance is not an issue because the voltage does not change. The capacitance associated with the top interconnect is important since the voltage needs to be switched. This capacitance is at least an order of magnitude below that of the bottom integration pad and interconnect because the interconnect is smaller and has an additional layer of 3 to 5 μm thick polyimide insulation over the overglass that separates the interconnect from the conductive silicon substrate. Some circuit designs, however, require low capacitance at both terminals of the RTD, which requires an improved process. Another drawback of the current process is the need for substantial post-

processing after bonding of the thin-film RTD die, which becomes more challenging when integrating multiple RTDs.

Next-Generation RTD Fabrication

An improved RTD fabrication process was in development at the end of the program. It is designed to lower the parasitics capacitance associated with hybrid integration. In addition to the front- and back-contacted RTDs that were integrated into CMOS circuits, several RTD structures were included that located both RTD terminals on the front of the die. This allows for RTD integration without the post-processing required to contact the back of the RTD component. Figure 3.4-1 illustrates the current integration technique compared with the front-contacted technique. The process uses proven IC fabrication technology based on the nanoelectronic integrated circuits previously fabricated at Raytheon. The process flow for a basic front-contacted RTD is outlined in Figure 3.4-2, with the layout view shown in Figure 3.4-3.

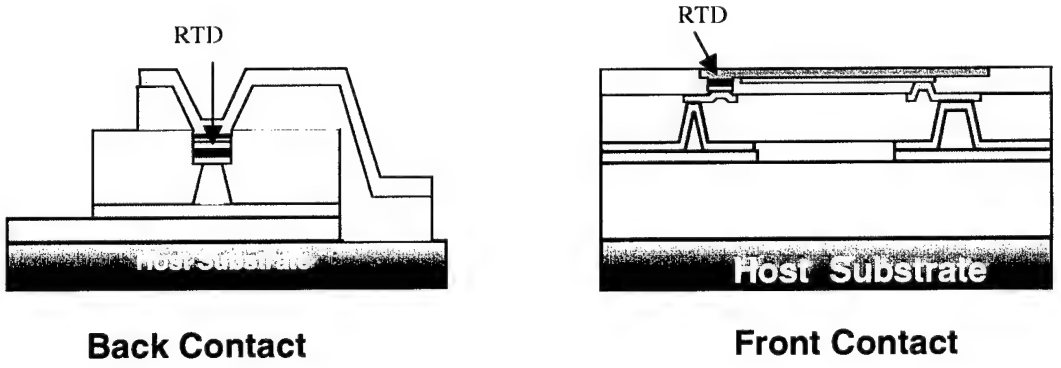


Figure 3.4-1. The back-contact RTD integration scheme currently in use as compared with the next-generation structure. Both RTD terminals contacted on the front of the wafer.

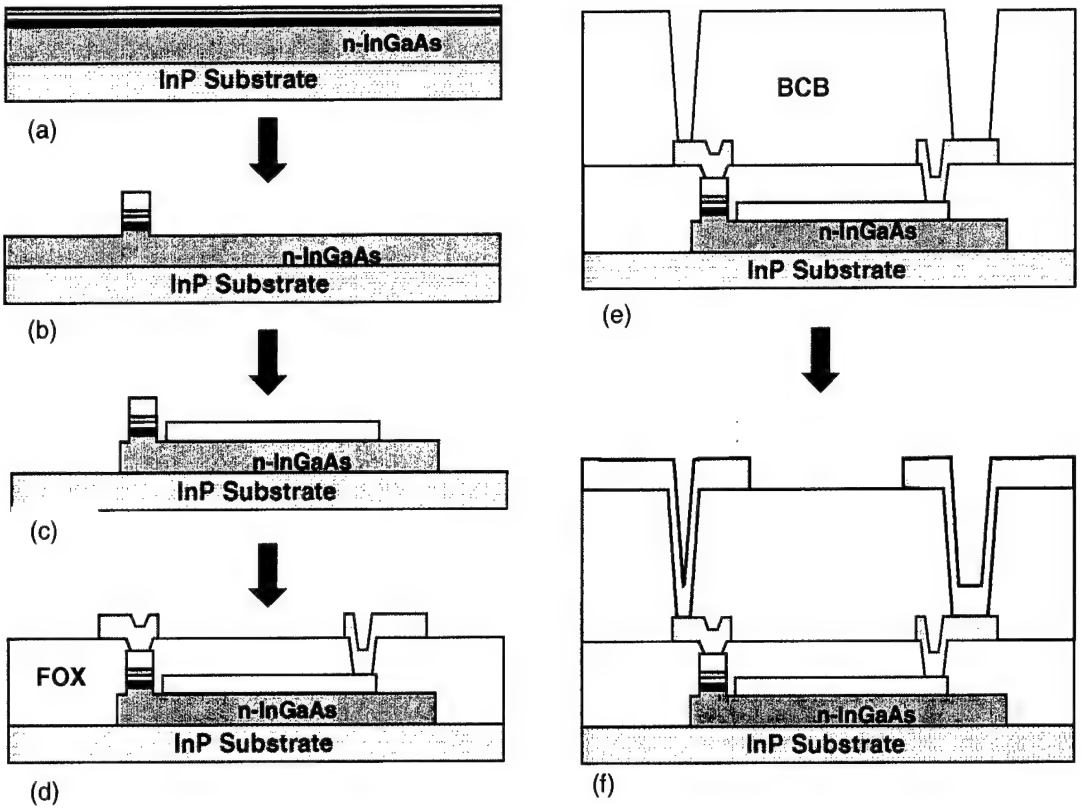


Figure 3.4-2. The next-generation RTD fabrication process flow. (a) The initial epitaxial structure. (b) The Ti/Pt/Au RTD top contact is patterned, followed by a self-aligned etch of the InGaAs. (c) The ohmic contact to the bottom n-InGaAs layer is evaporated, followed by a mesa etch of the n-InGaAs layer to the substrate. (d) The FOX passivation layer is deposited, followed by the via etches to the RTD and ohmic contact. The Metal 1 layer is then sputtered and patterned. (e) The BCB Level 2 planarizing dielectric is spin-coated and cured. Vias are etched to Metal 1. (f) Metal 2 is sputtered and patterned to complete the process.

Besides allowing for an all-front-contacted process as shown in Figure 3.4-2, the on-wafer InP RTD fabrication process was modified to incorporate the added improvements listed below.

Process Improvement	Benefit
5× optical stepper's improved alignment tolerance	Allows minimum-geometry RTDs to be fabricated (1.4× 1.4 μm)
n-InGaAs mesa etch	Reduces overlap of top overlying metal and n-InGaAs layer
FOX passivation/Level 1 dielectric	1.0 μm thick layer lowers dielectric capacitance, with improved degree of planarization over Si_3N_4
BCB Level 2 dielectric	Planar top surface and mechanical stability

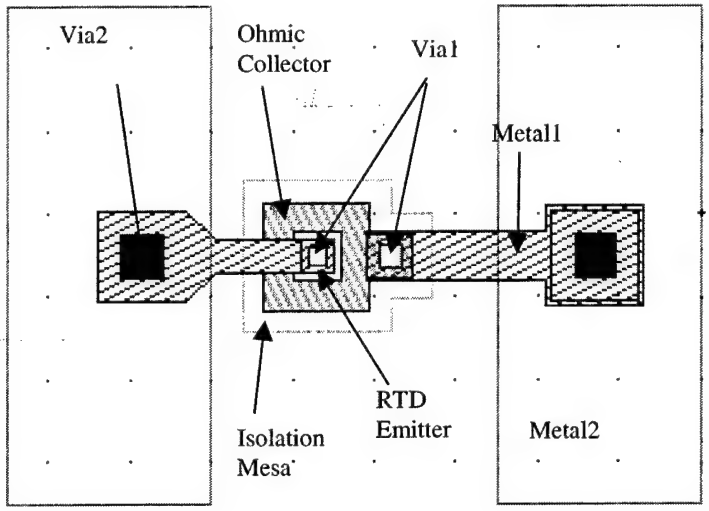


Figure 3.4-3. Layout view of front-contacted RTD (60×95 μm).

Included in the mask set for the next-generation RTD fabrication are structures for multiple RTDs that are commonly used in RTD/CMOS circuits, as listed below, and described in Figure 3.4-4. Each of the structures listed below is available in four different RTD areas: 1.4×1.4 μm^2, 2×2 μm^2, 4×4 μm^2, and 6×6 μm^2.

Structure	Number of RTDs	Number of Terminals	Type of Contact (Back or Front-only)
Single RTD	1	2	Back
Single RTD	1	2	Front-only
Asymmetric RTD Pair	2	3	Front-only
Symmetric RTD Pair	2	3	Front-only
Independent RTD Pair	2	4	Front-only
RTD Bridge	4	4	Front-only

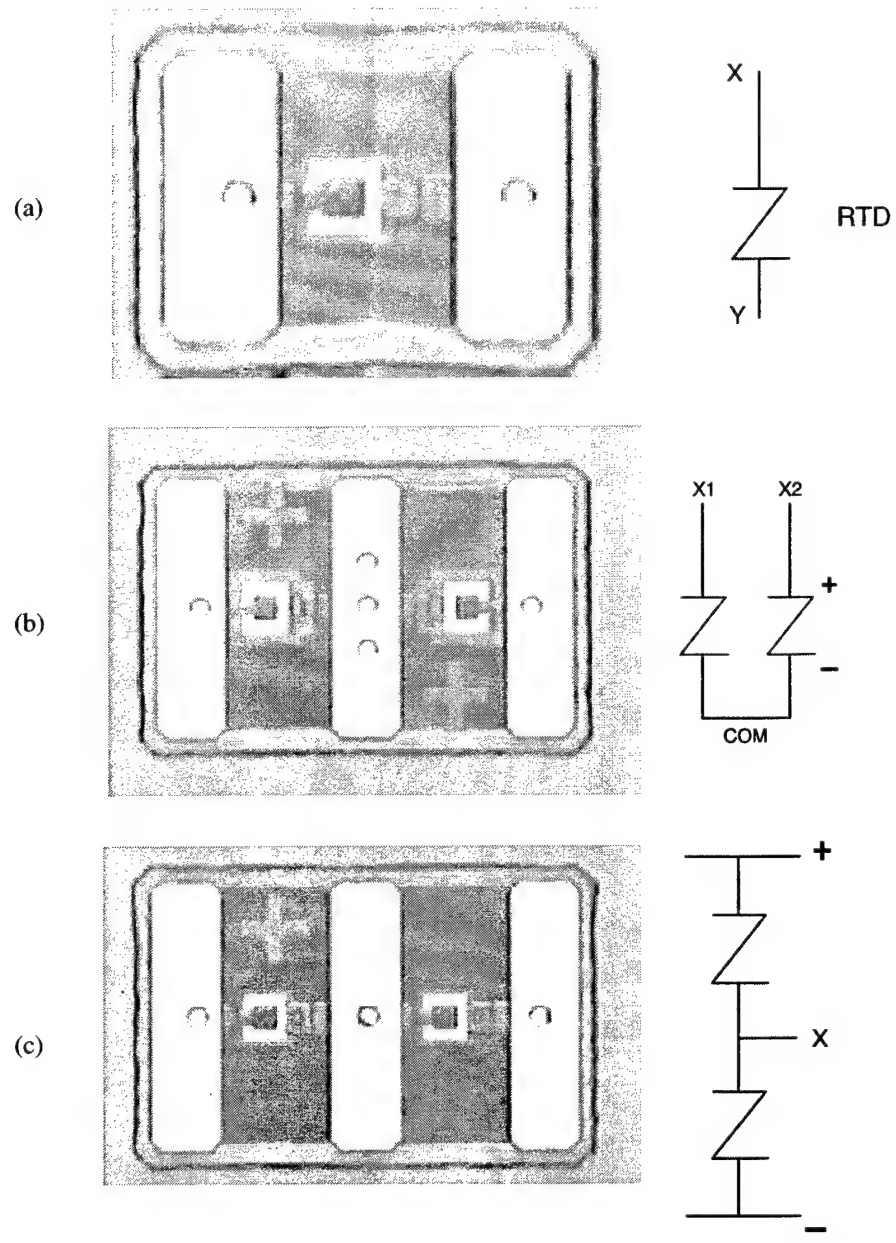
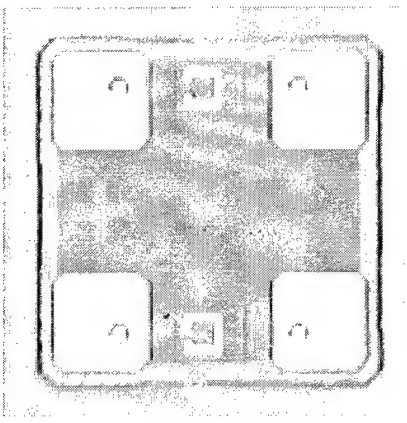
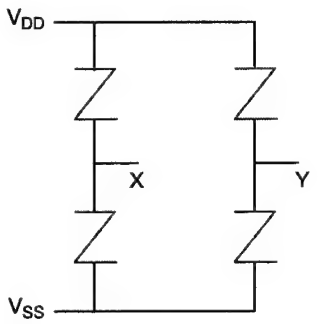


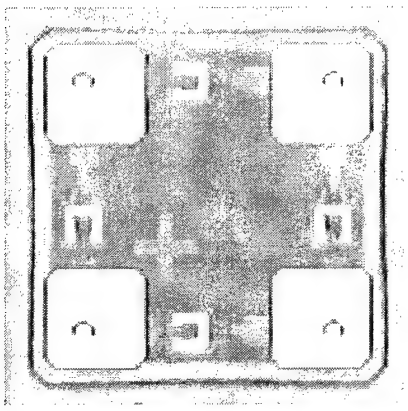
Figure 3.4-4. The RTD structures included in the next-generation mask set: (a) single RTDs, (b) symmetric RTD pair, (c) asymmetric RTD pair, (d) independent RTD pair, and (e) RTD bridge.

(d)





(e)



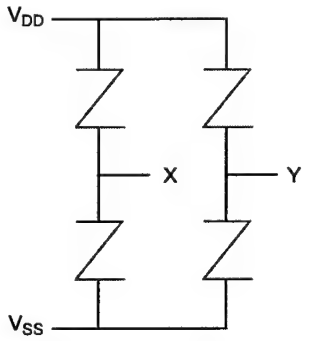


Figure 3.4-4. (Continued) The RTD structures included in the next-generation mask set: (a) single RTDs, (b) symmetric RTD pair, (c) asymmetric RTD pair, (d) independent RTD pair, and (e) RTD bridge.

Step A. Epitaxial Growth [Refer to Figure 3.4-2 (a)]

Five 3-inch InP substrate epitaxial wafers were grown using solid source molecular beam epitaxy (MBE). To vary the RTD peak current density, the epitaxial layer structure of each wafer used a different barrier thickness. The peak current density ranged from 0.5 to 60 kA/cm^2. Shown in Figure 3.4.5 is a typical RTD layer structure; the only variation between wafers was the inclusion and thickness of a lattice-matched InAlAs pre-barrier to lower the peak current density. The 100 Å n-InP layer served as an etch-stop.

Step B. RTD Emitter Patterning [Refer to Figure 3.4-2 (b)]

The RTD mesa itself was patterned using a self-aligned etch process in which the RTD top contact serves as the etch mask. The contact was fabricated using a nitride-assisted liftoff

technique, in which a 3000 Å Si_3N_4 layer was deposited by PECVD before photoresist was spun and patterned. After photolithography, the nitride was etched and undercut to assure a clean liftoff. The wafers were exposed to a brief argon sputter etch and then a 100 Å TiW sputter deposition, all while in a high vacuum to ensure a clean metal-semiconductor junction for a good ohmic contact. A Ti/Pt/Au/Ti layer of 400/400/2800/600 Å was evaporated before the resist was lifted off in acetone. The Si_3N_4 layer is removed.

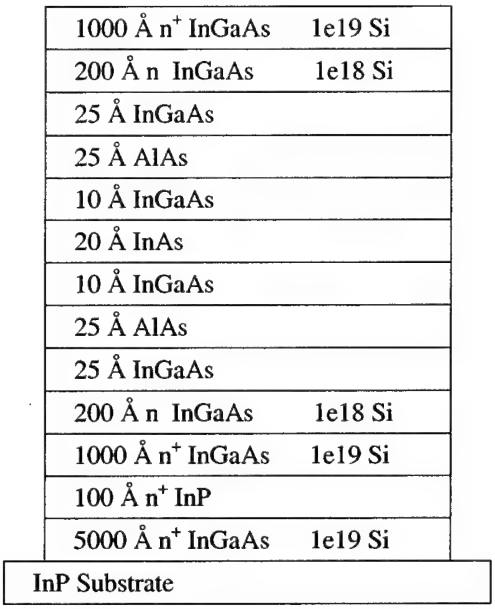


Figure 3.4-5. The layer structure of the RTDs fabricated. All layers except InAs and AlAs are lattice-matched to InP.

The dimensions of the RTDs are 1.4×1.4, 2×2, 4×4, and 6×6 μm square. To achieve the minimum geometry scaling, anisotropic dry etching must be employed to pattern the RTDs. Due to the difficulty of RIE etching of indium-based semiconductors, ablative ion milling was employed to etch approximately 1800 Å through the RTD. The ion mill process is selective enough between Ti and InGaAs to ensure that the contact is not severely eroded in the process. As can be seen in Figure 3.4-6, excellent scaling was achieved, with little undercut. In addition, good etch depth uniformity was achieved across the wafer.

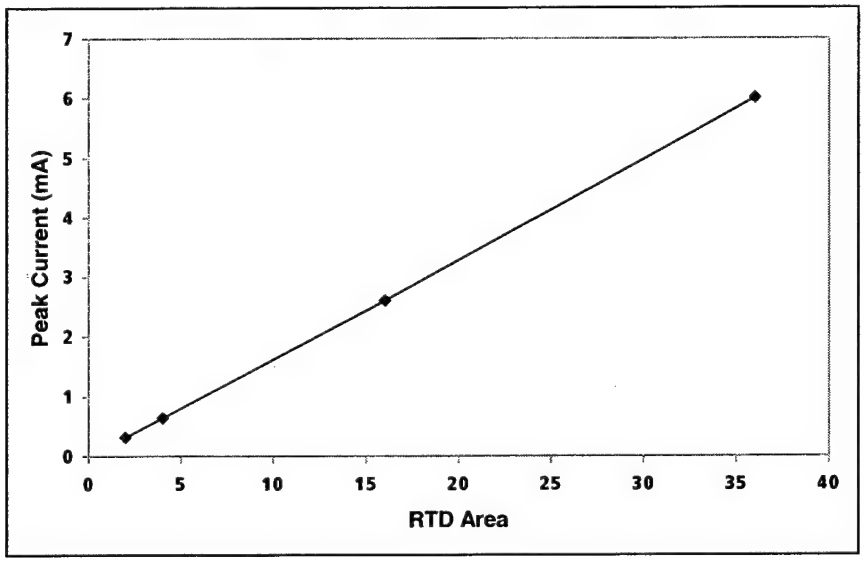


Figure 3.4-6. The scaling of RTD peak current with layout area shows no lateral undercut.

Step C. Ohmic Collector Contact and Isolation Mesa [Refer to Figure 3.4-2 (c)]

The second contact to the RTD was made using the same liftoff process as the emitter (top) contact. Subsequently, an isolation mesa was patterned with conventional lithography. Because the layout design rules allowed for a large overlap of the active area, considerable undercut could be tolerated. For this reason, wet chemical etching in 1:8:160 (H_2SO_4: H_2O_2: H_2O) was used to etch the isolation mesa.

Step D. FOX Dielectric and Metal1 [Refer to Figure 3.4-2 (d)]

For passivation, a 400 Å Si_3N_4 layer was deposited with PECVD. A partially planarizing layer of FOX was deposited to a total thickness of 1.0 μm. Vias to the RTD were patterned with optical stepper lithography, with a minimum dimension of 1.0 μm. The vias were etched in a CHF_3/O_2 RIE that results in a slightly sloped sidewall (for better metal step coverage).

The Metal 1 layer of TiW/Au/TiW was sputtered to a thickness of 1500/4000/400 Å. After patterning the Metal 1 mask with photolithography, the metal layers were etched, using CF_4/O_2 RIE to etch the TiW and ion milling to etch the Au.

Step E. BCB Level 2 Dielectric and Via 2 Etch [Refer to Figure 3.4-2 (e)]

Before the BCB polymer was spun, a thin (400 Å) Si_3N_4 layer was deposited to improve adhesion between the BCB and the underlying TiW and FOX. The BCB resin was subsequently spun to 2.4 μm and cured at 250 °C for 1 hour. BCB was used as the Level 2 dielectric because of its low parasitic properties (K = 2.7) and its excellent planarization properties (>90% degree of planarization).

Because BCB is an organic polymer, a photoresist was eroded in the BCB RIE. For this reason, a 1000 Å TiW etch mask was sputtered before Via 2 lithography. The pattern was etched in the TiW mask with CF_4/O_2 RIE. To etch the vias, an O_2/CF_4 plasma etch was employed with high pressure to give a sloped and undercut sidewall profile. The TiW mask is removed with a wet chemical etch in hydrogen peroxide.

Step F. Metal 2 Patterning [Refer to Figure 3.4-2 (f)]

The Metal 2 layer that composes the large bond pads was composed of TiW/Au/TiW sputtered to a thickness of 1000/5000/400 Å. The reduced TiW thickness was employed to reduce the stress associated with Metal 2. Metal 2 was etched in the same way as Metal 1.

Step G. Final Thin-Film Mesa Etch

The last step before substrate removal was the etch of the BCB and FOX around the RTD structure to isolate each thin-film structure so that each one could be independently transferred. In this case, a TiW mask could not be used because it would be eroded in the FOX RIE. Instead a 1000 Å layer of Al was evaporated over a 200 Å TiW barrier layer. After the mask was patterned, the BCB and FOX were etched all the way down to the InP substrate using the same etch methods as those used in previous steps. The Al and TiW were subsequently removed with wet chemical etching.

Stress-Related Problems

Subsequent to the stripping of the resist after patterning Metal 2, cracks were observed in the BCB. Thorough experimentation showed that the crack formation occurred in the top surface of the BCB and propagated outward from the corners of the Metal 2 pattern, indicating

that stress between the TiW and the BCB was the cause of the cracking. The cracks formed after exposure to the oxygen plasma that was used to strip the resist. To eliminate the cracking, the following process modifications were employed:

Used wet resist stripper only after BCB was deposited, avoiding all exposure to plasma

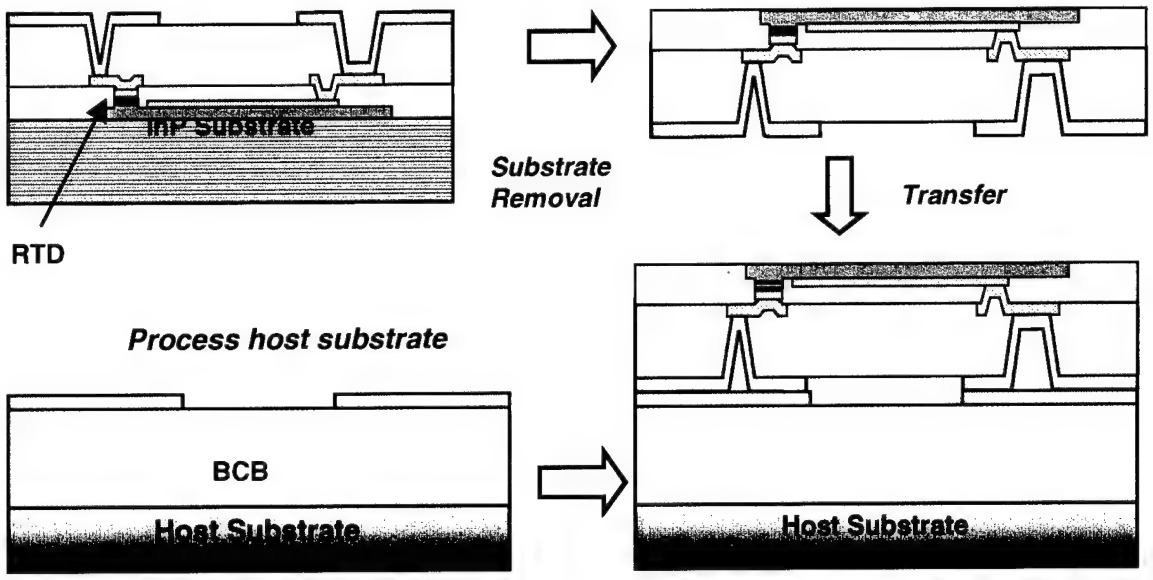
Used only 1000 Å TiW in the Metal 2 tie layer so as to lower the associated stress

Added scribe lines to the Via 2 pattern so that if cracks formed in isolated areas, they would not propagate far

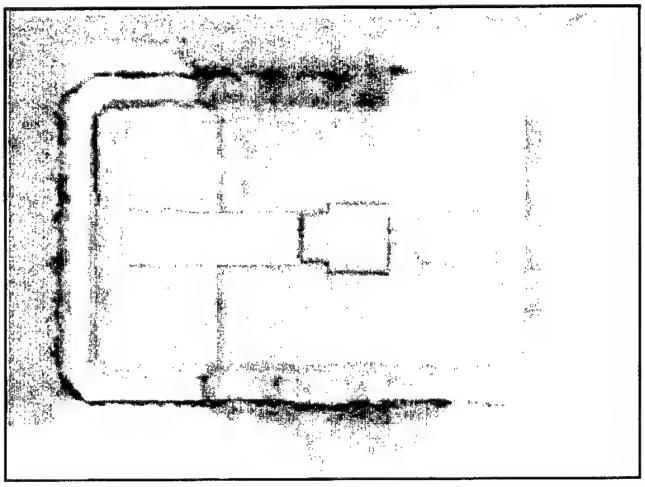
Filleted the corners of both the Via 2 and Metal 2 patterns from 90 to 45 degrees to lower the stress associated with the corners.

Substrate Transfer

The substrate transfer process described in Section 3.3 can be readily modified to the fabrication of next generation of low-parasitic RTDs. Such a modification is shown in Figure 3.4-7. The substrate removal procedure is entirely unchanged, but there is a slight modification in the host substrate pre-transfer processing. To lower the parasitic capacitance to the conductive p-Si substrate present in CMOS, an additional insulating layer is applied. In our case, we use 5 μm thick BCB because of its low parasitics and excellent planarization. The other difference is that both contact pads are located on the front side. The transfer process is illustrated in Figure 3.4-6 (a), with a photomicrograph of a finished integrated RTD on silicon shown in Figure 3.4-6 (b).



(a)



(b)

Figure 3.4-7. The modified thin-film integration method (a) is shown, along with a finished thin-film RTD integrated onto silicon.

3.5 Characterizing the Parasitics of the Hybrid Process

Achieving the highest circuit performance required the reduction of all sources of parasitic capacitance. Overall parasitic capacitance due to presence of the thin-film RTD was ascribed to four fundamental contributions, regardless of the type of integration process used

(front-only contacts or back-contacted): (1) device, (2) thin-film structure, (3) integration interconnect, and (4) CMOS pad capacitance. Figure 3.5-1 shows an integrated RTD structure with each component of the parasitic capacitance identified.

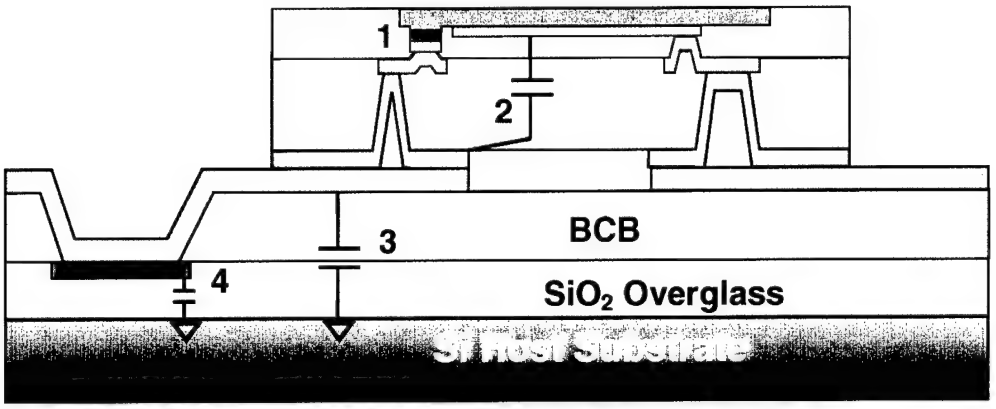


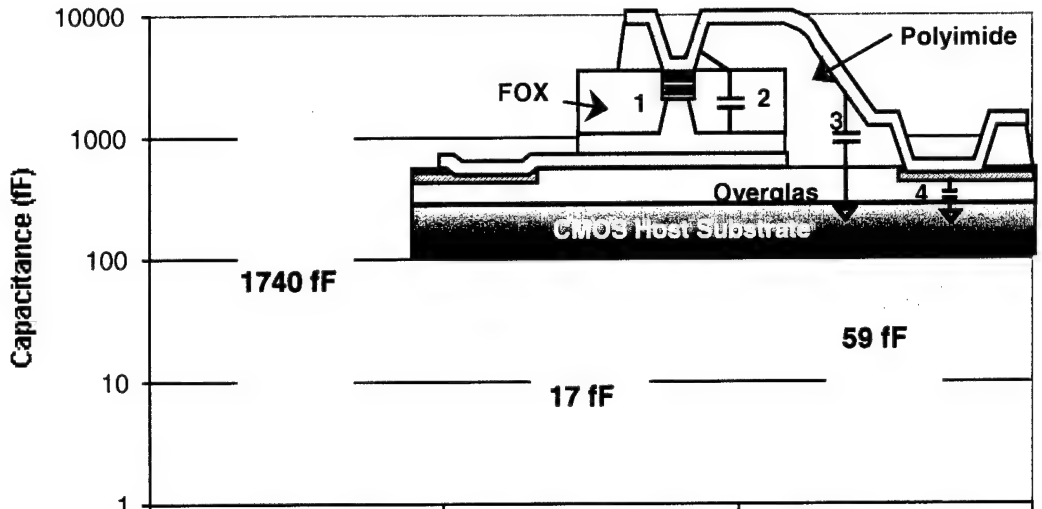
Figure 3.5-1. The components of the overall parasitic capacitance: (1) device capacitance, (2) dielectric capacitance in the thin-film structure, (3) interconnect capacitance to the substrate, and (4) CMOS pad capacitance.

The measured RTD junction capacitance ranged from 2 to 8 fF/μm^2, depending on the specific quantum heterostructure. The fundamental improvement in device capacitance was achieved by scaling down the RTD area from a minimum of 16 μm^2 in the original RTD process to a minimum of 2 μm^2 in the new set. This improvement was made possible by the transition from contact print lithography to optical stepper lithography, and the corresponding improvement in alignment tolerance.

The capacitance associated with the thin-film RTD structures was very high due to the thin 500 Å Si_3N_4 layer. This contribution to the capacitance can be reduced to negligible levels by using the FOX passivation process. Connection to the RTD is made through a via in a planarizing 1 μm oxide over layer. Vias as small as 1.0 μm can be etched in the FOX, allowing a via directly to the top of the RTD, resulting in very low dielectric capacitance from Metal 1 to the back n-InGaAs layer. Also, the n-InGaAs bottom layer is etched to form a mesa that has minimal overlap with the overlying metal layers, further reducing the capacitance associated with the thin-film structure.

The interconnect and CMOS pad capacitance depend upon how the RTD is integrated onto the CMOS chip. In the back-contacted process of Figure 3.4-1, the top interconnect is insulated from the conductive silicon substrate (typically 1 to 100 ohm-cm) by both the overglass and the polyimide interlayer dielectric, resulting in a low parasitic interconnect. The improvement in parasitic capacitance could only be achieved by reducing the size of the interconnect, resulting in interconnect capacitances of less than 5 fF. The bottom integration pad, due to the lack of the polyimide layer for insulation and the larger size of the pad, had a parasitic capacitance on the order of 50 fF, which is too large to serve as an output node. For this reason, in the front-contacted process of Figure 3.4-1, the interconnects could not be formed directly on the overglass, even though the interconnects were smaller than the large bottom integration pad in the back-contacted process. Rather, an additional layer of insulation, a BCB layer 3 to 6 μm thick, was applied to the CMOS chip before transfer of the RTD die. Vias to the CMOS pads were first etched in the cured BCB layer, and the gold integration pads were patterned on over the BCB, as can be seen in Figure 3.5-1. The capacitance of the CMOS pad was strictly a function of the pad area. A safe size of 40 × 40 μm was chosen in early designs, but a transition to 20 × 20 μm pads is in progress, reducing the pad capacitance to below 4 fF.

Figure 3.5-2 shows a comparison of the overall capacitance of an integrated RTD in both the original and next-generation back-contacted RTD process. The rather high capacitance associated with the original structure is dominated by the capacitance through the 500 Å Si_3N_4.



	Prototype 4x4 (fF)	Optimized 1.4x1.4 (fF)	Optimized 4x4 (fF)
4) CMOS Pad	16	4	4
3) Interconnect	20	2.9	2.9
2) Dielectric	1656	4.4	4.4
1) Device	48	6	48

Figure 3.5-2. The distribution of the total parasitic capacitance for the integrated RTD structure. The large capacitance in the prototype integration method is due to the thin 500 Å nitride separating the n-InGaAs back contact and the Ti/Au contact.

The overall estimated capacitance distribution is detailed in Figure 3.5-3 for the single front-contacted RTD for the four different device sizes included in the next-generation RTD mask set. The capacitance was dominated by the devices sized greater than $2 \times 2\,\mu m^2$. Figure 3.5-4 details the overall capacitance per interconnect with minimum geometry RTDs for several different structures included in the mask set. Figure 3.5-5 shows how the simulated power consumption of a comparator design varies with the output capacitance at the RTD, illustrating the importance of this parameter in reducing the parasitic capacitance.

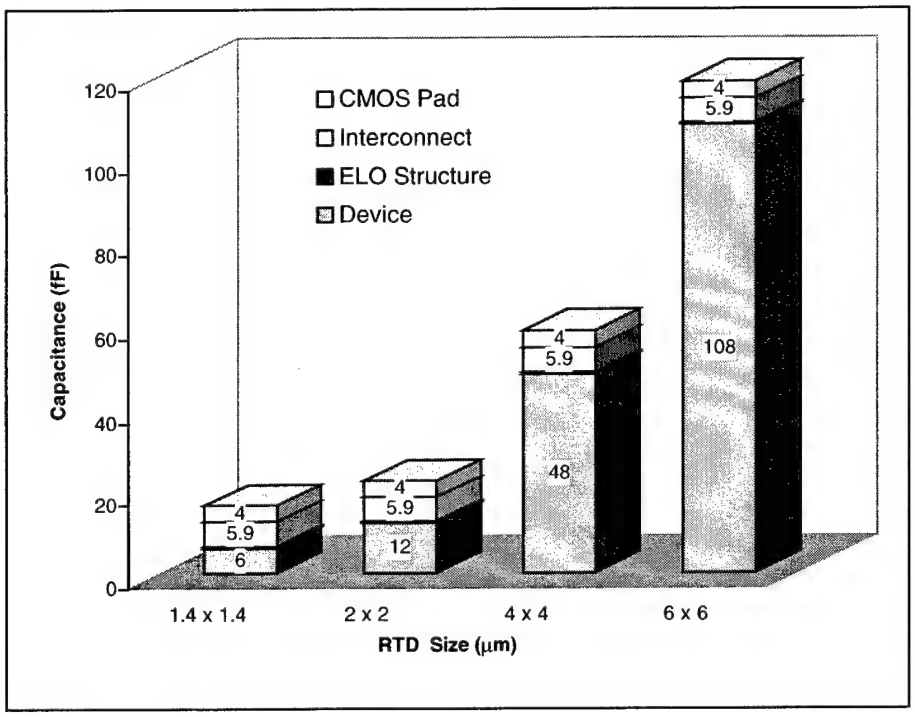


Figure 3.5-3. The overall capacitance of the integrated front-contact RTD, with each component shown individually. The ELO structure's contribution is less than 0.5 fF. The device capacitance clearly dominates for RTDs larger than minimum geometry.

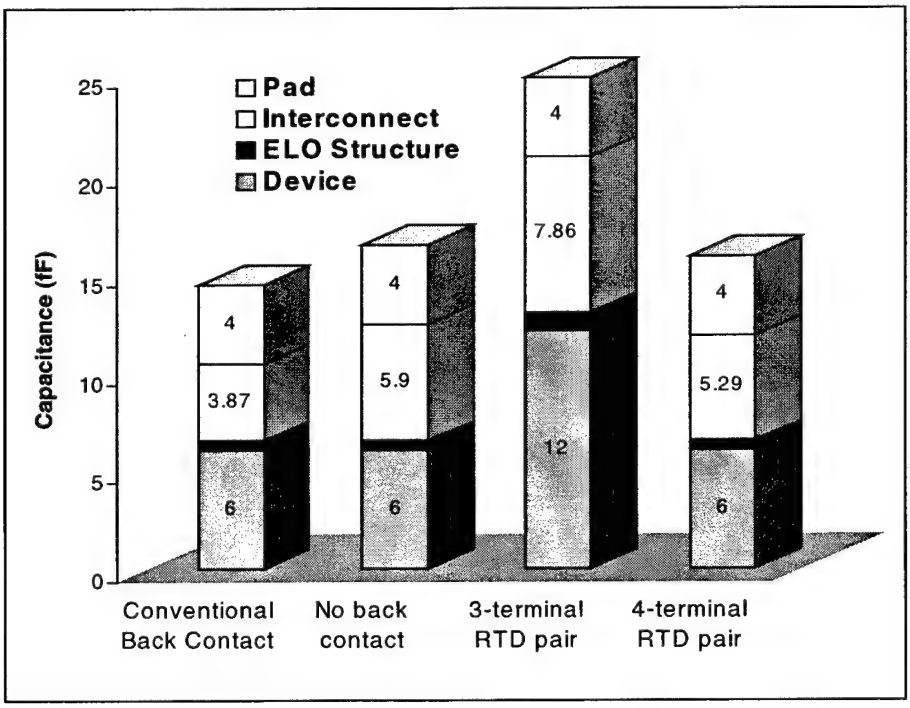


Figure 3.5-4. The distribution of capacitance per interconnect for several structures. Two RTDs share a single interconnect in the three-terminal pair (asymmetric).

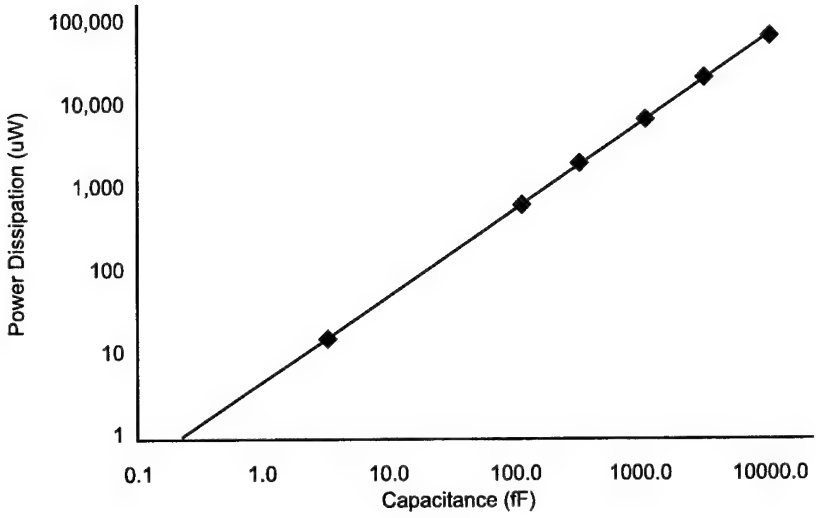


Figure 3.5-5. The power dissipation of various RTD/CMOS comparator designs for different output capacitances, operating at a speed of 1.5 Gsps.

4. DEVICE AND CIRCUIT TEST RESULTS AND COMPARISON WITH PREDICTIONS

4.1 Comparator Simulation

The RTD-CMOS comparator circuit shown in Figure 4.1-1 represents the first known demonstration of planarized integrated thin-film RTDs onto CMOS circuits. In addition, the circuit has improved switching characteristics as compared to the all-silicon equivalent. The function of the current mode RTD/CMOS comparator is to produce a large change in output voltage for a small change in input current. Such a circuit is ideal for sensitive analog-to-digital conversion functions, including optical receiver applications, in which an optical detector generates small changes in current as digital information is received. In this circuit, current source biases the RTD just below its switching point so that the RTD can be switched between two states. In the binary 0 state, the detector (emulated as a current source in Figure 4.1-1) is not illuminated and does not supply current to the circuit. The RTD in this condition is bistable, with two stable operating points at the same current level but different voltages. Because the comparator is reset before the input changes, the RTD remains biased just below its switching threshold. In the binary 1 state, the detector is illuminated and injects a small amount of current, which is just enough to increase the current through the RTD above its threshold current. In this state the RTD is monostable, and it switches to the only stable operating point at a high voltage level. When the current is lowered, the RTD will remain latched in the high-voltage state until it is reset. The voltage difference across the RTD between the two states is just enough to drive an inverter, which brings the RTD response up to the proper logic levels. Figure 4.1-2 shows the RTD current-voltage characteristic used for simulating the DC operation of the RTD/CMOS comparator. Figure 4.1-3 shows the operation of the RTD/CMOS comparator with the RTD.

The integrated comparator is shown in Figure 4.1-4. The sinusoidal input was provided by an arbitrary waveform generator. The voltage source is translated into a near sinusoidal current by the current mirror, which provides a resistive load to the waveform generator. In this circuit, the nMOSFET is clocked to externally reset the RTD. The circuit, as shown in Figure 4.1-4, is externally biased with a source measurement unit to a power supply voltage of 5 V.

When the injected current from the input causes the total RTD current to exceed its peak current, the circuit latches to the high voltage state. The RTD I-V characteristic is shown in Figure 4.1-5. The external clock resets the comparator to the low voltage state. The response of the circuit with a sinusoidal input is shown in Figure 4.1-6. The response agrees well with simulation. The sinusoidoidal input is superimposed on the unbuffered output. This feedthrough can be removed by including a CMOS output buffer. The abrupt transition of the output is clearly shown at the threshold voltage of 1.1 V, allowing the comparator to be used as a high-sensitivity threshold comparator.

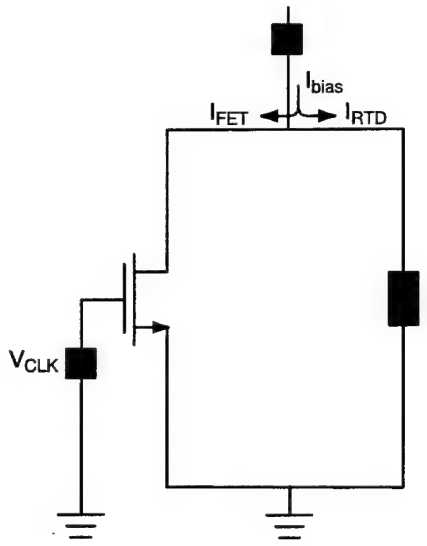


Figure 4.1-1. The RTD/CMOS Comparator Circuit. When the V_{CLK} is on, the nFET quenches the RTD by pulling most of the current. The RTD is set to its low-voltage state.

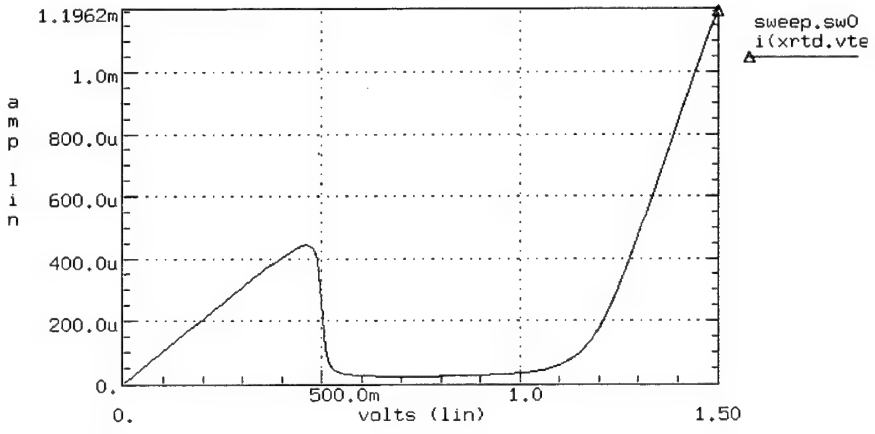


Figure 4.1-2. RTD current-voltage characteristic used for the simulation.

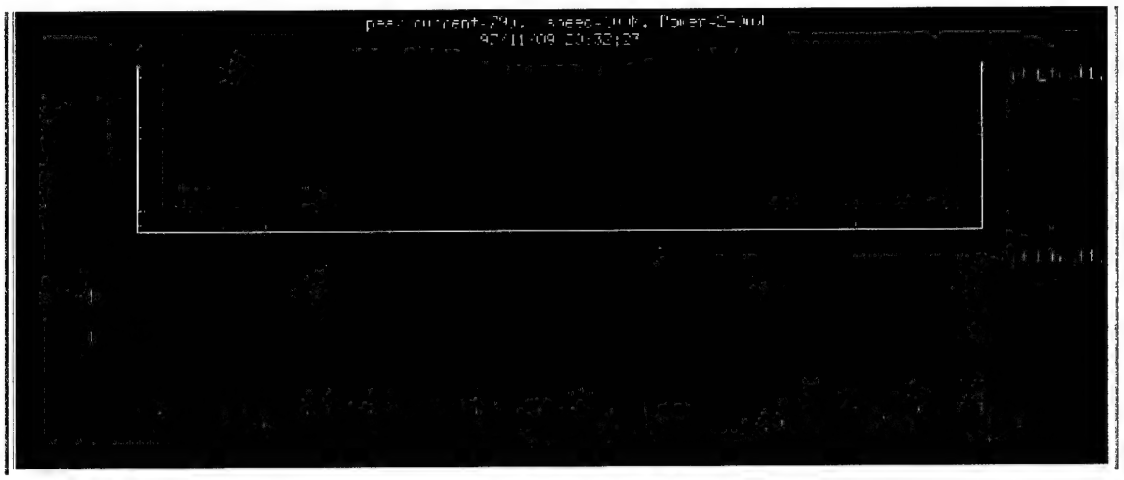


Figure 4.1-3. Simulation of comparator with an RTD whose DC characteristics are shown in Figure 4.1.2.

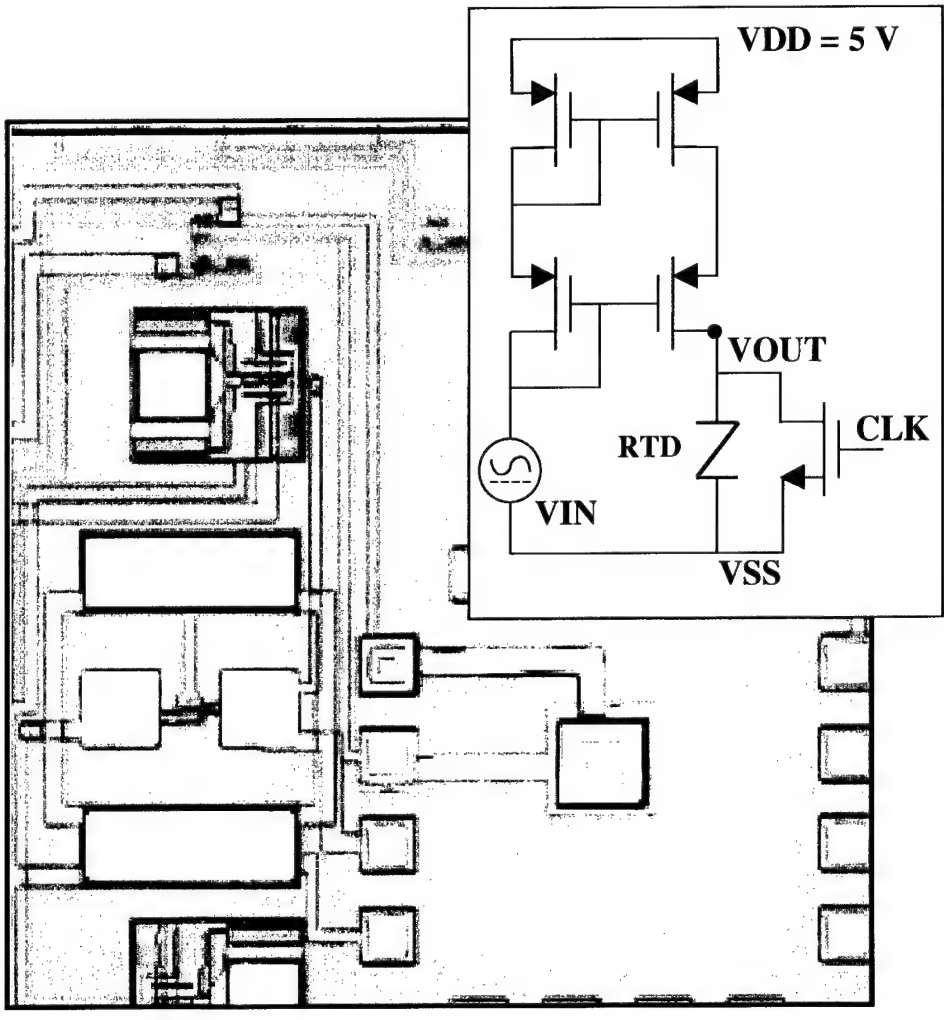


Figure 4.1-4. An Integrated RTD/CMOS Comparator. The RTD die measures 95 × 95 μm, with a 16 μm diameter RTD. The circuit schematic is shown in the inset.

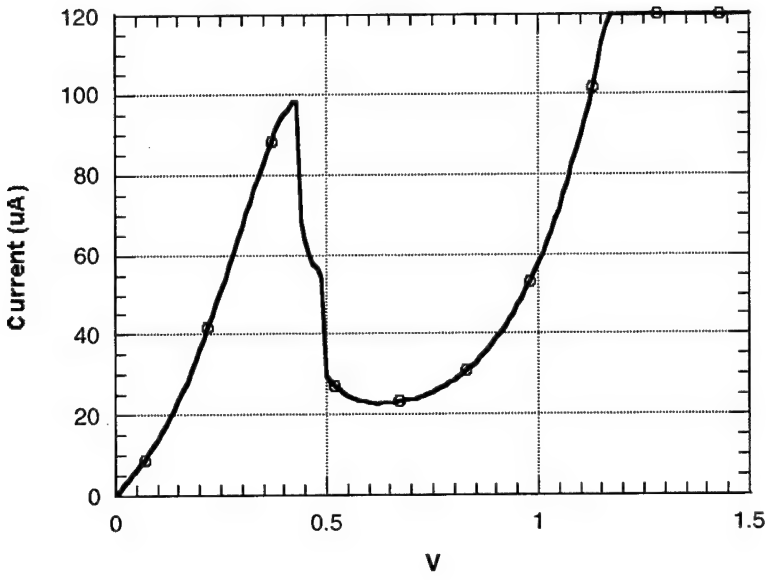


Figure 4.1-5. NDR of RTD integrated with the comparator whose results are shown in Figure 4.1.6.

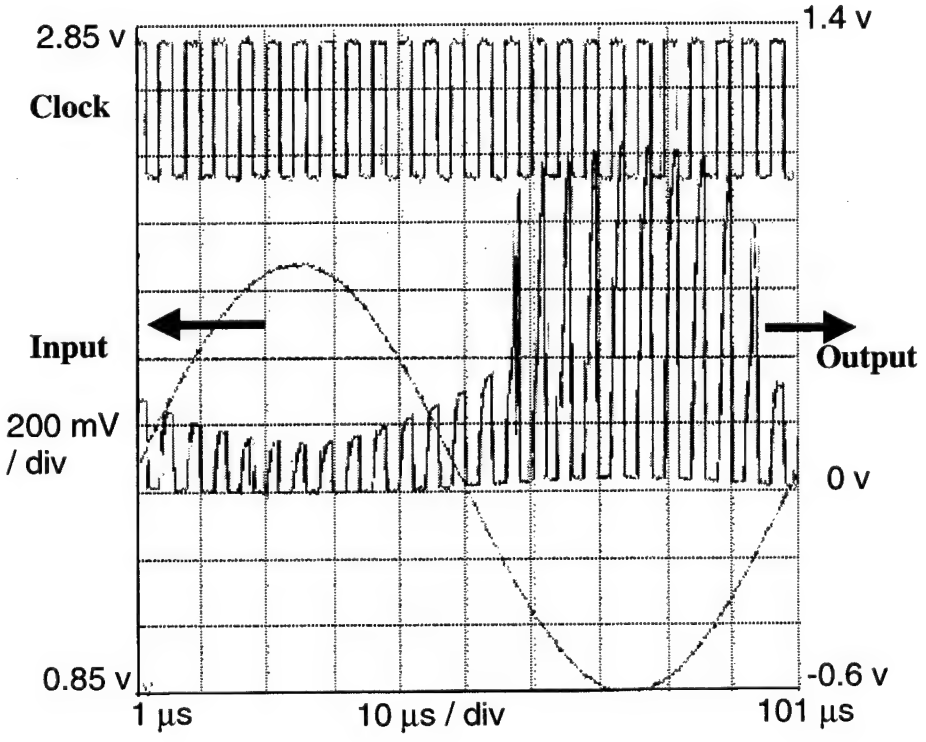


Figure 4.1-6. Transient operation of the RTD/CMOS comparator shown in Figure 4.1-4

4.2 NMOS/RTD Building Blocks: Schmitt Trigger and Transimpedance Amplifier

In addition to the comparator, we demonstrated nMOS/RTD building blocks including a Schmitt trigger and transimpedance amplifier. These circuits also showed greatly reduced component counts over comparable all-CMOS designs. The circuit configuration of the inverting Schmitt trigger and transimpedance amplifier are shown in Figure 4.2-1 (a) and (b), respectively.

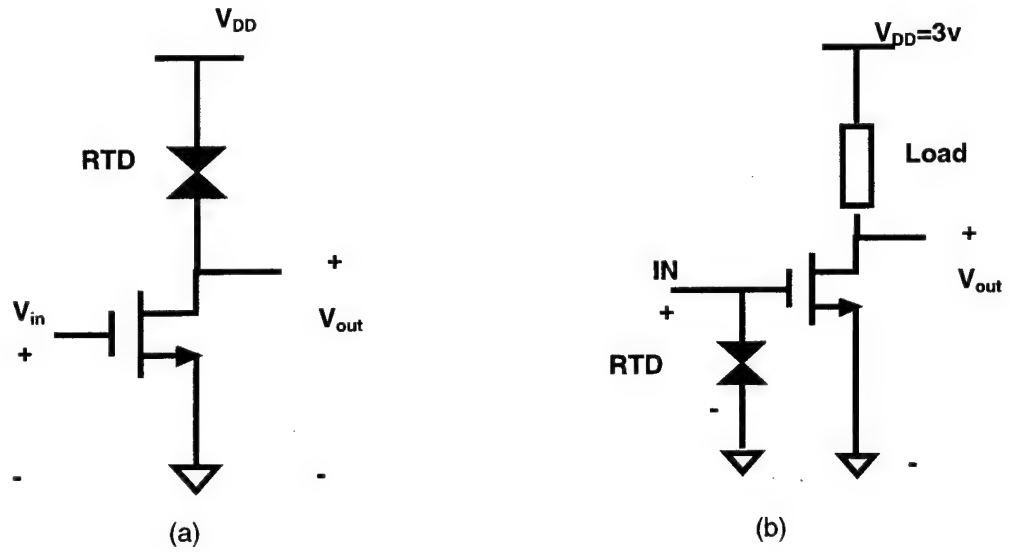


Figure 4.2-1. The (a) Schmitt trigger and (b) transimpedance amplifier circuits.

The Schmitt triggered inverter is the most basic example of a threshold logic circuit. When the input voltage is increased, the current pulled through the RTD by the nFET increases accordingly, and when this current exceeds the RTD peak current, the output voltage switches to the high state of the RTD and latches. Similarly, when the input voltage is decreased, the current to the RTD is lowered, resulting in a switch to the RTD's low-voltage state when the current falls below the RTD's valley current. In a digital circuit, there are at least two nMOSFETs, and when a certain number of the MOSFETs are on, the RTD's peak current is exceeded and the circuit switches state. In this way, multiple input NAND, NOR, and majority gates can be compactly realized. In the case of the Schmitt inverter circuit implemented here, the margin is determined by the peak-to-valley ratio (PVR) of the RTD and the relative match between the RTD current and the current drive capability of the nFET. The integrated RTD

characteristics of the RTD/nFET Schmitt trigger are shown in Figure 4.2-2 (a), with the measured transfer curve shown in Figure 4.2-2 (b).

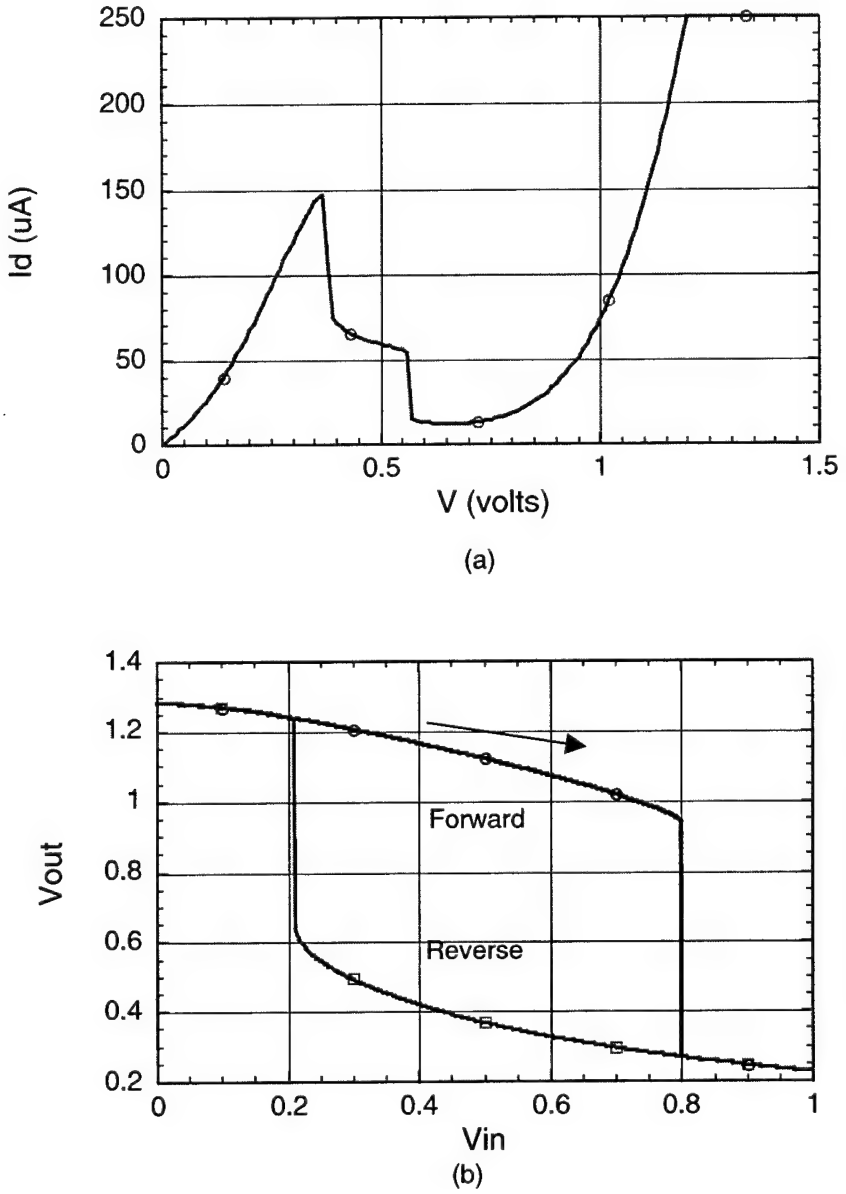


Figure 4.2-2. (a) The integrated RTD I-V characteristics; (b) the transfer curve of the RTD/nFET inverting Schmitt trigger.

The transimpedance amplifier shown in Figure 4.2-1 (b) takes advantage of the RTD's transition between stable states. When the injected current into the RTD exceeds its peak

current threshold, the RTD switches to its high-voltage state, which is above the nFET's threshold voltage of approximately 0.7 V. The measured transfer curve is shown in Figure 4.2-3 (a) and compares well with the simulated curve shown in Figure 4.2-3 (b).

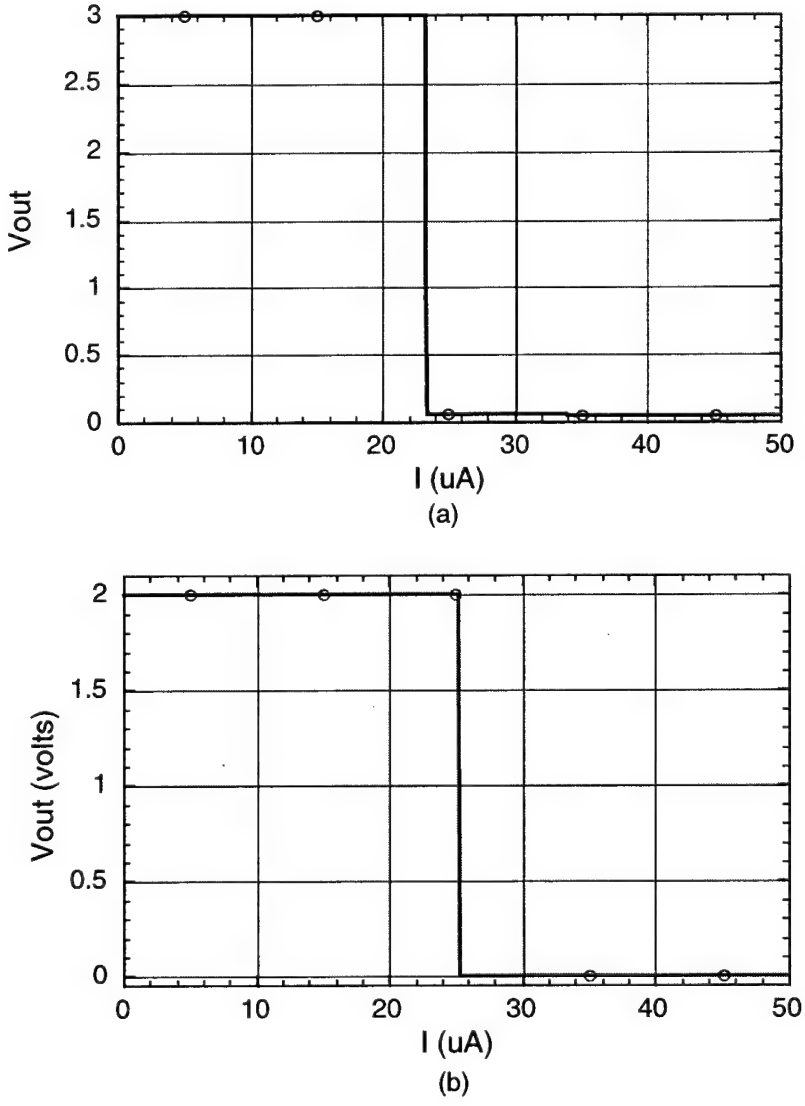


Figure 4.2-3. (a) The measured transfer curve of the RTD/nMOS transimpedance amplifier agrees well with the simulated curve (b).

4.3 Submicrometer RTD Arrays

Arrays of submicrometer RTDs were transferred to silicon substrates using the thin-film transfer process detailed in Section 3. In addition to studying the potential of integrating arrays, this investigation demonstrates the feasibility of using Raytheon's FOX passivation and planarization process for future thin-film structures. Multiple arrays of 1, 10, 100, 1000, and 10,000 RTDs in parallel were transferred. The RTD device areas ranged from 0.1×0.1 μm^2 to 1.0×1.0 μm^2, available in all of the array sizes mentioned above. The characteristics of the transferred substrate RTDs, shown in Figure 4.3-1, for 0.4×0.4 μm^2 RTDs were not significantly altered from their pre-processed response. In general, the current of the RTD array was lowered very slightly, but the peak-to-valley current ratio (PVR) was not degraded.

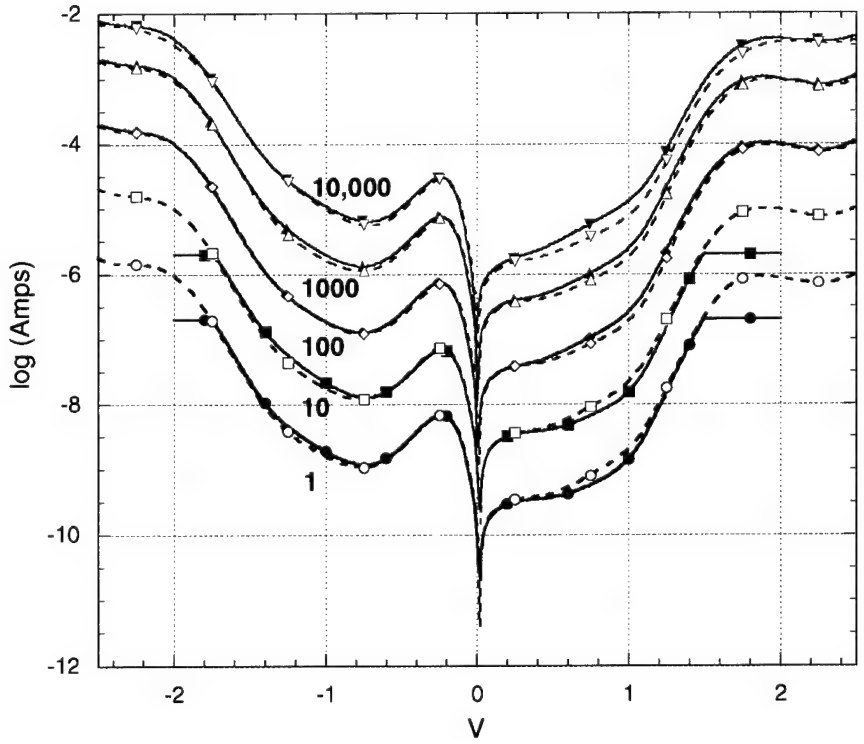


Figure 4.3-1. I-V Characteristics of the 0.4×0.4 μm^2 RTD Arrays. The solid lines indicate the on-wafer characteristics, while the broken lines indicate the characteristics after substrate transfer and bonding.

4.4 Transferred Substrate HBTs

Initial experiments were made on HBTs transferred to silicon by the epitaxial liftoff technique. Preliminary DC, RF, noise, and load pull characterization of substrate transferred HBTs showed little to no degradation in performance. In some cases, DC gain and maximum power-added efficiency of these devices showed slight improvement. More thorough investigation of HBTs transferred onto high thermal conductivity substrates such as beryllia and diamond could be used to determine if the better heat sinking of the silicon substrate accounts for the increase in gain efficiency of HBT-on-silicon power amplifiers. To our knowledge, these represent the first measurements on transferred substrate HBTs.

Figures 4.4-1 through Figure 4.4-4 demonstrate the preliminary measurements taken on devices on the original InP substrate and ELO devices on quartz and sapphire. The measurements provided here are a comparison of devices on the original InP and devices from the same wafer that were ELO onto quartz and sapphire. By measuring a large enough sample within the wafer, the results of these measurements can be further validated.

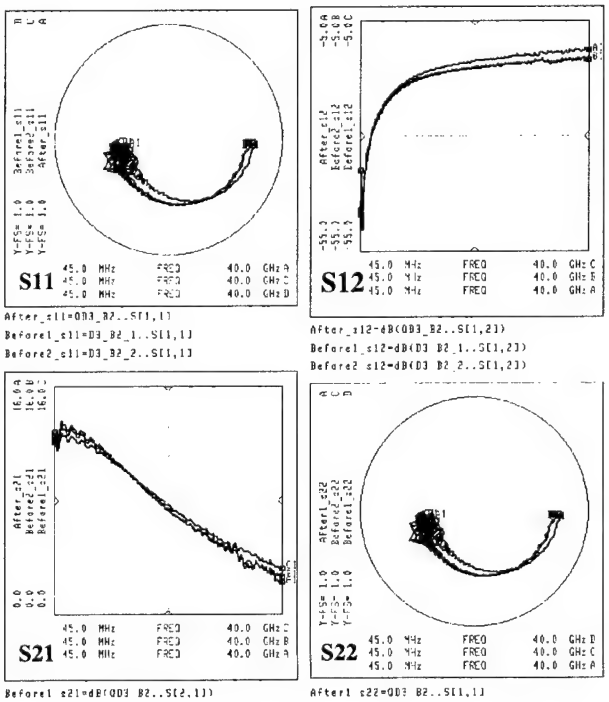


Figure 4.4-1. Small signal characteristics of an HBT on its original InP substrate and ELO devices on quartz.

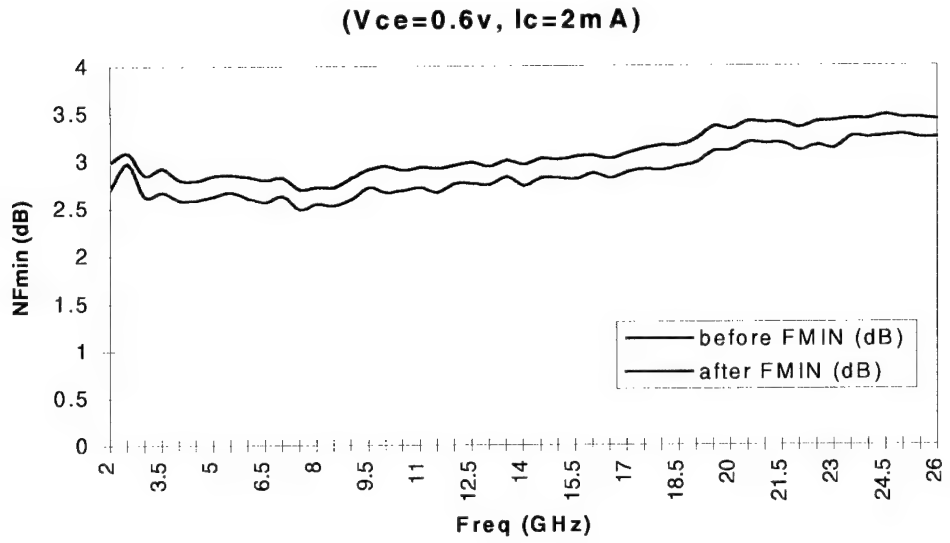


Figure 4.4-2. Noise figure of HBT on its original InP substrate and ELO devices on quartz.

A slight shift in the S-parameters was observed, as shown in Figure. 4.4-1, but no degradations in gain were caused by this shift. Noise figure was degraded very consistently across the frequency spectrum by a measure of 0.2 dB, attributable to the substrate removal and transfer.

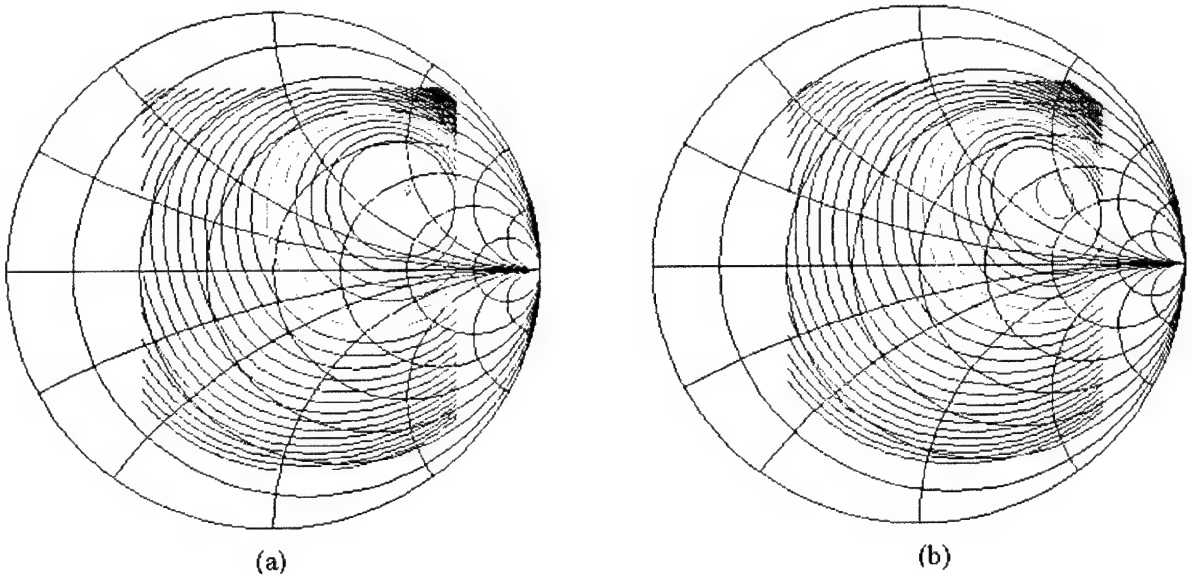


Figure 4.4-3. Load contours of HBT (a) on the original InP substrate and (b) ELO devices on quartz.

Load pull measurement of numerous devices produced a consistent demonstration of little or no change in performance due to ELO. As shown in Figure 4.4-3, the maximum power-added efficiency occurs at about the same load-matching condition, and large signal characteristics of the devices are unchanged. In addition to no change in the load gamma of maximum power-added efficiency, no significant changes were observed in its value, as illustrated in Figure 4.4-4.

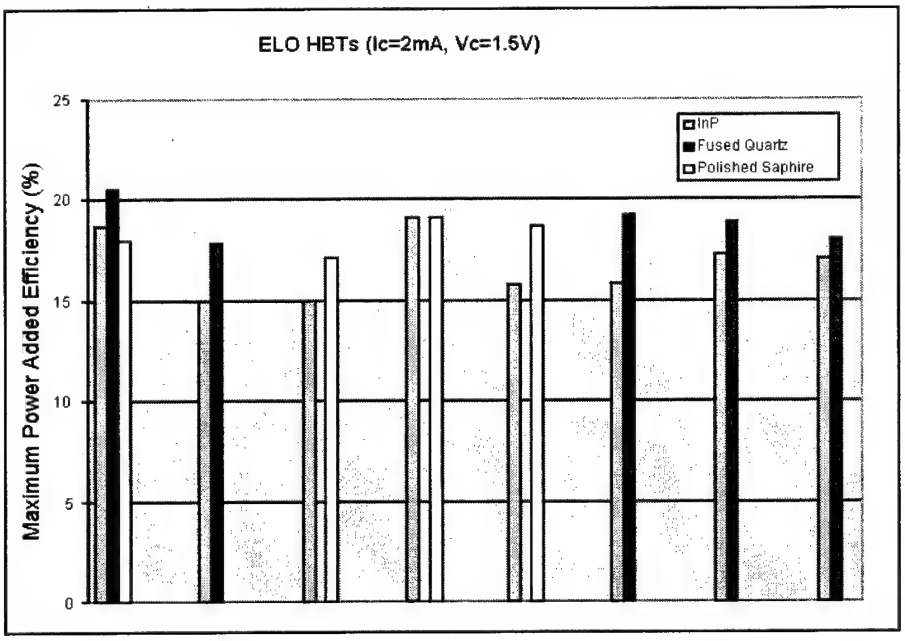


Figure 4.4-4. Maximum power-added efficiency of HBTs on their original InP substrate and ELO devices on quartz and sapphire at 9 GHz. Each column represents a different transistor geometry from the same processed wafer.

4.5 Low-Parasitic Thin-film RTDs Transferred to Silicon

Towards the end of the program, we successfully transferred and bonded thin-film, low parasitic RTDs. These structures differ from the conventional planarized RTD structures used previously in that they have been optimized to reduce the parasitic capacitance associated with the transferred RTD structure to levels below the device capacitance intrinsic to the RTD. This is done by etching an isolation mesa in the n-InGaAs back contact layer around the RTD and all the way down the semi-insulating InP substrate. Thus, the overlap between the metal and the n-InGaAs contact layer is minimized, lowering the capacitance.

These structures are also front-contacted, similar to a flip chip, in which all bond pads are on the top surface of the chip to be flipped and bonded. For the conventional planarized RTDs, there is a broad area pad that is aligned and bonded, with the need for substantial post-processing to provide an interconnect and contact to the backside terminal of the RTD. The new approach is illustrated in Figure 4.5-1. In addition to facilitating the integration of single-RTD structures, multiple-RTDs structures can be transferred and integrated without increased process complexity.

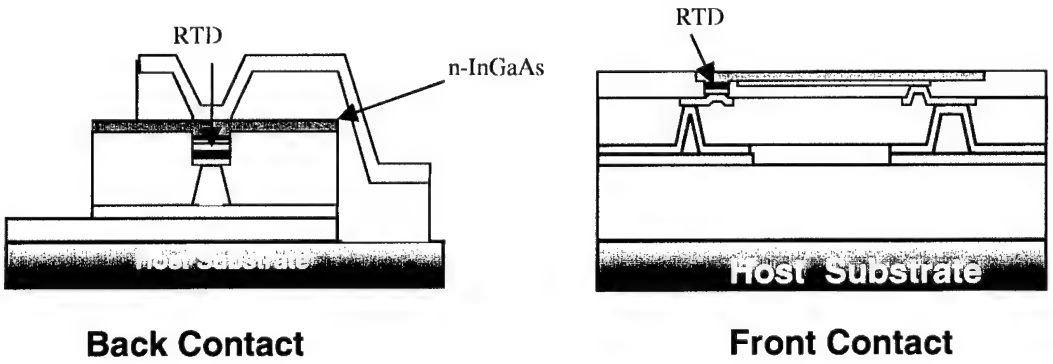


Figure 4.5-1. A cross-sectional view of the conventional back-contact integration scheme and the new front-contacted integration method. Note the presence of a large overlap area between the back-contact n-InGaAs layer and the metal pad.

A die of the next-generation, low-parasitic RTDs was separated from the InP growth substrate and transferred to pads on silicon using the alignable transfer process mentioned earlier and detailed in the following section. Results are shown after thin-film integration for a single RTD and a series RTD pair in Figure 4.5-2. There is no noticeable shift in the I-V characteristics resulting from the substrate transfer process.

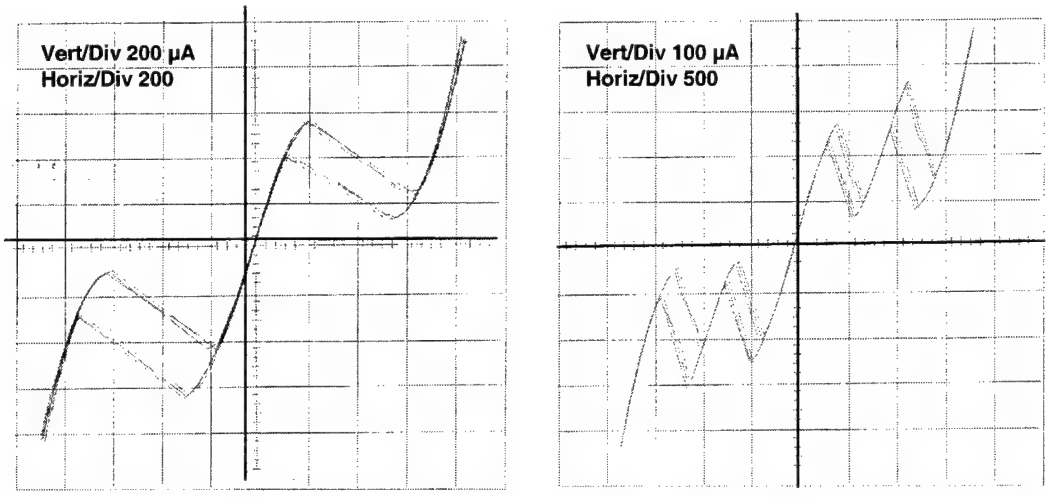


Figure 4.5-2. DC characteristics of thin-film, integrated, next-generation RTD structures: (a) single RTD, and (b) two connected RTDs.

5. SUMMARY AND CONCLUSION

Epitaxial substrate transfer methods were developed and used to demonstrate hybrid RTD-CMOS circuits. This hybrid integration technology offers the advantage of being able to combine devices and circuits of different materials in a manner that improves performance relative to either material alone. A major benefit of hybrid integration is that both circuits or devices can be independently optimized using mature fabrication processes.

A broad suite of circuits were fabricated and evaluated for logic, memory, optoelectronic, and mixed-signal applications. In general, we found that the class of mixed-signal circuits such as A/D converters are well suited to hybrid RTD-CMOS technology. These circuits offer significant improvement over all-CMOS designs in terms of speed-power product, due to the RTD's inherently high switching speed and bistable operation. Because of the relatively large sizes of the devices and interconnects used in the transferred substrate process, we did not observe a major speed improvement in comparison to that of the best dynamic CMOS logic designs. In any such technology, whether it be flip chip or epitaxial substrate transfer, considerable further development of the bonding process itself is necessary to ensure that the parasitics associated with the hybrid integration do not cancel out the advantage of using two different technologies. Based on computer simulations, however, a truly monolithic (that is, epitaxial) RTD/CMOS technology would provide a significant improvement in speed and power efficiency for logic functions. For example, latched low-power RTD pairs could be used to offset leakage in dynamic CMOS designs and thereby dramatically lower refresh and standby power requirements. Another advantage of a monolithic RTD/CMOS process lies in the fundamental improvement in circuit density that could be achieved in digital logic without shrinking device dimensions. This alone would result in greater speeds and/or lower power and cost.

We conclude that mixed-signal RT-CMOS circuits have performance advantages for niche applications in the short term, and broad use in logic when silicon-based RT technology reaches process maturity.

APPENDIX

RTD/CMOS Nanoelectronic Circuits: Thin Film InP-Based Resonant Tunneling Diodes Integrated with CMOS Circuits

The manuscript "RTD/CMOS Nanoelectronic Circuits: Thin Film InP-Based Resonant Tunneling Diodes Integrated with CMOS Circuits" is in press with *IEEE Electron Device Letters.*

APPENDIX

The manuscript "RTD/CMOS Nanoelectronic Circuits: Thin-Film InP-Based Resonant Tunneling Diodes Integrated with CMOS Circuits" was published in the March 1999 edition of *IEEE Electron Device Letters.*

RTD/CMOS Nanoelectronic Circuits: Thin-Film InP-Based Resonant Tunneling Diodes Integrated with CMOS Circuits

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Abstract -- The combination of resonant tunneling diodes (RTDs) and complementary metal-oxide-semiconductor (CMOS) silicon circuitry can offer substantial improvement in speed, power dissipation, and circuit complexity over CMOS-only circuits. We demonstrate the first integrated resonant tunneling CMOS circuit, a clocked one-bit comparator with a device count of 6, compared with 21 in a comparable all-CMOS design. A hybrid integration process is developed for InP-based RTDs which are transferred and bonded to CMOS chips. The prototype comparator shows sensitivity in excess of 10^6 V/A, and achieves error-free performance in functionality testing. An optimized integration process, under development, can yield high- speed, low- power circuits by lowering the high parasitic capacitance associated with the prototype circuit.

I. INTRODUCTION

The ongoing need for improved speed and density in high-performance multifunctional electronics has motivated extensive research into the transfer and bonding of electronic and optoelectronic devices to host substrates, including silicon [1-5]. Hybrid thin-film integration of III-V devices onto CMOS circuitry is a promising technique which has been successfully applied to optoelectronic circuits, allowing each component to be independently optimized with proven technologies at relatively low cost [6-8].

The resonant tunneling diode (RTD) is well known for its intrinsic bistability and high-speed switching capability due to negative differential resistance (NDR). The NDR characteristic has been exploited in novel digital integrated circuits combining RTDs and transistors, enabling greater functionality than transistor-only circuits, including digital logic [9, 10] and low-power, high-density memory cells operating at room temperature [11]. Functional density can be further improved by using vertically stacked RTDs in multistate memory and logic [12, 13]. Analog circuits are also achievable, and a prototype 4 bit, 2 Gsps flash-ADC has been implemented [14].

The inherent bistability of the RTD eliminates the need for circuit feedback in comparators, with switching time limited only by the capacitive load on the RTD. With reported switching times of 1.5 ps [15], comparators operating at 20 Gbps clock rates are possible. The high gain of the RTD NDR allows conversion from the analog input signal to the digital domain in one stage. The RTD has been used in several high-speed analog front-end circuits, including oscillators, mixers, frequency multipliers, and RF detectors [16-19].

We have developed a process to integrate III-V resonant tunneling devices with conventional CMOS circuitry and have recently demonstrated the world's first resonant tunneling CMOS circuit: a clocked one-bit comparator. The resonant tunneling devices are fabricated on an InP substrate and transferred to a CMOS die using a thin-film transfer and bonding process. These prototype circuits are being used to evaluate the advantages of tunnel devices in CMOS circuit topologies and help in defining the roadmap for monolithic resonant tunneling CMOS ICs with the advent of an integrable silicon resonant tunneling component.

II. FABRICATION AND EXPERIMENTAL PROCEDURE

Chk fig refs.The RTD layers were grown using molecular beam epitaxy on an InP growth substrate. A cross-sectional view of the RTD structure is shown in Figure 1(a). The $In_{0.53}Ga_{0.47}As$/InAs/ $In_{0.53}Ga_{0.47}As$ quantum well serves to increase the peak-to-valley ratio (PVR) by increasing the separation between quasibound resonant states due to the lower effective mass of InAs over InGaAs, and by lowering the first resonant voltage. The barriers are formed by two symmetric $In_{0.52}Al_{0.48}As$/AlAs layers, which determine the peak current density. Although the use of InAlAs in the barrier reduces the PVR, it is employed because strain limits the thickness of the AlAs thickness to 25 Å, with peak current density reliably controlled by the thickness of the InAlAs pre-barrier [11]. For the RTDs that were integrated, a 30 Å pre-barrier results in a peak current density of 12 A/cm^2. The relatively low RTD peak current reflects the need to match the RTD current to the current drive capability of the CMOS circuitry.

After the RTD mesas are etched and a 500 Å Si_3N_4 passivation layer is deposited, a via is etched to the RTD mesa. A polyimide layer is spin-coated and cured. In addition to planarizing the top surface of the thin-film device for bonding, the 3 μm polyimide layer reduces the parasitic capacitance between the top contact and n-InGaAs bottom layer of the thin-film structure. A via surrounding the RTD mesa is etched in the polyimide by reactive ion etching (RIE), followed by contact patterning and a 200/4000 Å Ti/Au metallization. Subsequently, a self-aligned etch of the polyimide, Si_3N_4 passivation, and the 5000 Å bottom n-InGaAs layer isolates each RTD. The final on-wafer structure is shown in Figure 1(b), with only the InP substrate linking the RTDs. The InP substrate is removed by a combination of mechanical polishing and wet chemical etching with HCl. The RTD is then metal-to-metal bonded to a standard foundry CMOS circuit using an alignable thin-film integration process, as shown in Figure 1(c) [6]. Subsequent post-processing includes the application of a polyimide layer to serve as an interlevel dielectric and via etching to the RTD and the aluminum CMOS circuit pad. Finally, a second Ti/Au layer contacts the back of the flipped RTD die and connects the second RTD terminal to the CMOS circuitry. The thin-film RTDs show no degradation from the on-wafer characteristics, as seen in Figure 2(a).

The combination of an accurate RTD model and an integration process that preserves the device characteristics enables design optimization. The silicon circuitry was designed for foundry CMOS fabrication and was simulated using a physics-based model for the RTDs. A comparison of the measured and modeled I-V characteristics for a low current density RTD is shown in Figure 2(b).

III. RESULTS AND DISCUSSION

Several prototype CMOS circuits have been designed for integration with low current density RTDs. The prototypes include basic building blocks for low-power and high-speed circuit functions, including: multistate static access memory, tunneling binary SRAM, comparator, amplifier, and logic gates.

A prototype CMOS comparator was fabricated in an 0.8 μm foundry CMOS technology for integration with RTDs with peak currents below 200 μA. A photomicrograph of the integrated circuit is shown in Figure 3(a), along with the circuit schematic. The comparator function is achieved by a transition between the bistable states of the biased RTD, eliminating the need for more complicated circuitry in CMOS designs to provide positive feedback and latching. We find that the device count is reduced from 21 in an all-CMOS design to 6 in the RTD/CMOS design. The biasing network places the RTD in its low-voltage state, near the peak current. When the injected current from the input causes the total RTD current to exceed its peak current, the circuit switches to the high-voltage state and latches. The external clock resets the comparator to the low-voltage state. The response of the circuit with a sinusoidal input is shown in Figure 4. The response agrees well with simulation. The abrupt transition of the output is clearly shown at the threshold voltage of 1.1 V, allowing the comparator to be used as a high-sensitivity receiver. In addition to the comparator results reported, nMOS/RTD building blocks such as a Schmitt trigger and transimpedance amplifier have been demonstrated, also showing greatly reduced component counts over comparable all-CMOS designs.

To demonstrate improved performance over all-CMOS circuits, the RTD/CMOS integration process must be improved to lower the parasitic capacitance. An optimized process currently in development is shown in Figure 5(a). The RTD device capacitance itself is reduced by scaling the RTD area down from 16 μm^2 or more to 2 μm^2 and increasing the peak current density. The large capacitance through the 500 Å Si_3N_4 surrounding the RTD mesa can be eliminated by employing a thicker, planarizing Si_3N_4/SiO_2 dielectric for passivation instead of only Si_3N_4. The interconnect capacitance to the conductive silicon substrate is lowered by shortening the interconnect. Finally, the capacitance of the 40 × 40 μm aluminum pad to the

CMOS circuit is minimized by scaling the pad to 20 × 20 μm. The distribution of and estimated improvement in capacitance over the prototype process is illustrated in Figure 5(b).

IV. CONCLUSION

To our knowledge, these results represent the first demonstration of integrated nanoelectronics on silicon circuitry. Prefabricated InP-based RTDs have been integrated onto foundry CMOS circuits using planarization and thin-film integration processes to realize circuits with improved function and reduced device count. Basic analog and digital building blocks have been demonstrated: comparator, Schmitt inverter, and transimpedance amplifier. In addition, logic and static memory standard cell prototypes are in progress. Finally, a reduced parasitic integration process is under development which will provide high-performance nanoelectronic CMOS components.

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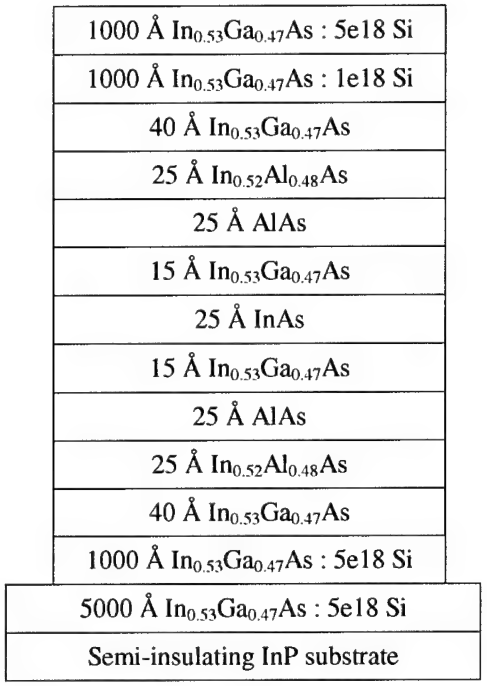
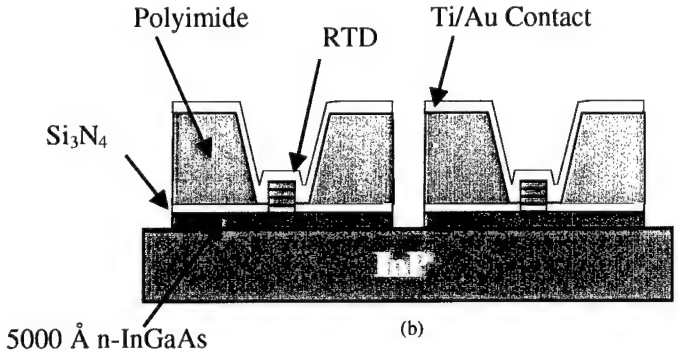


(a)



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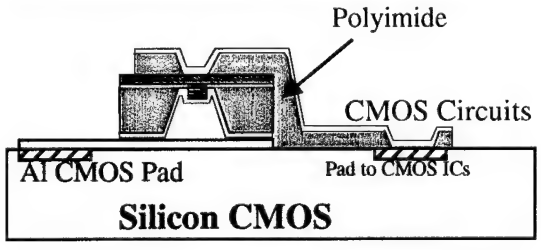
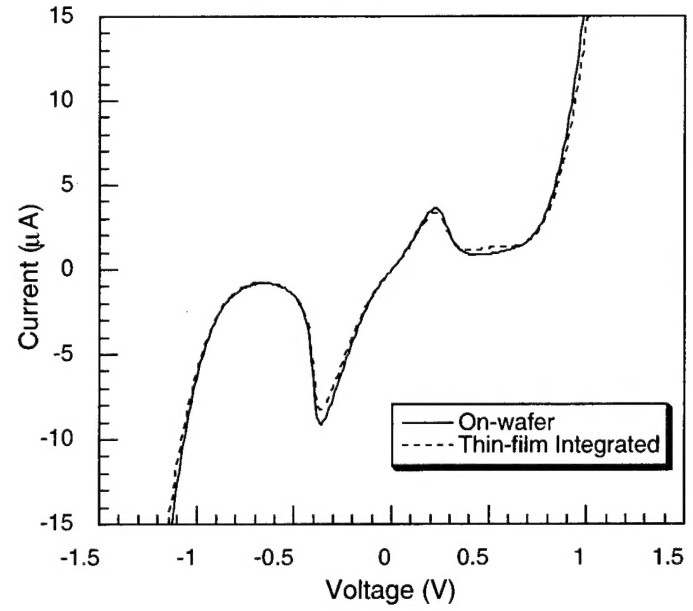


(c)

Figure 1. Thin-Film Integration of RTDs to CMOS. (a) The RTD layer structure as grown by molecular beam epitaxy. The planarized RTDs (b) are then individually isolated and separated from the InP substrate and aligned and bonded to the CMOS chip (c).



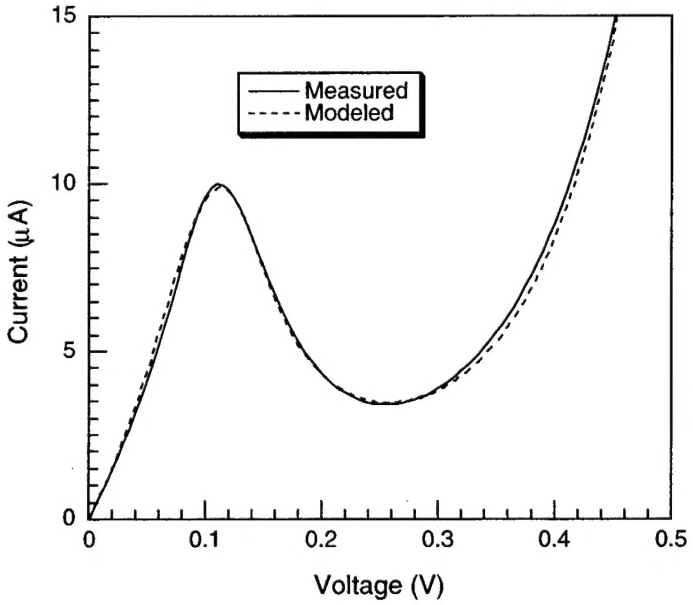


Figure 2. (a) On-wafer vs. fully integrated RTD I-V characteristics for a 36 μm^2 RTD, showing good agreement. (b) Measured vs. SPICE-modeled RTD I-V characteristics.

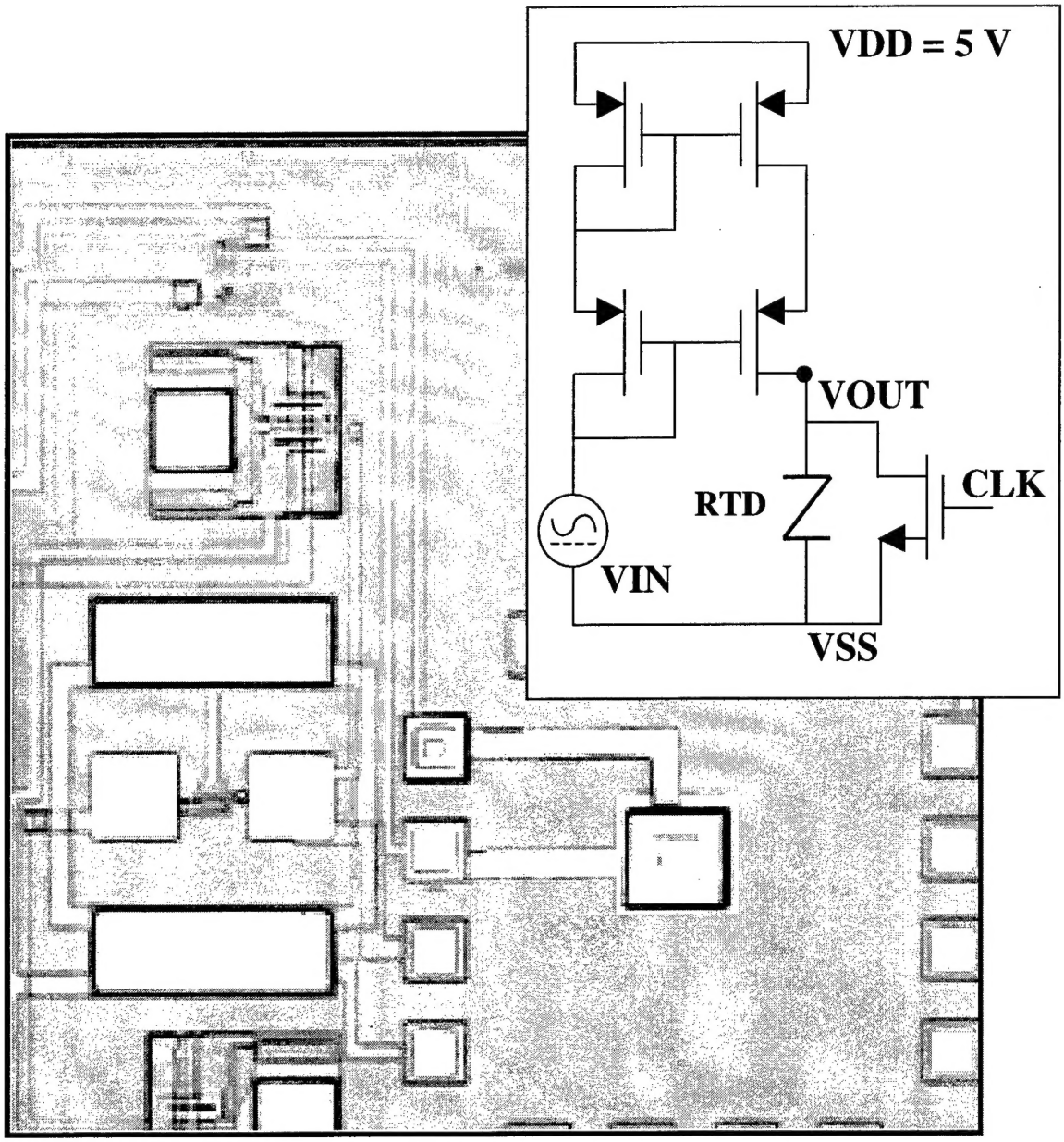


Figure 3. An Integrated RTD/CMOS Comparator. The RTD die measures 95 × 95 μm, with a 16 μm diameter RTD. The circuit schematic is given in the inset.

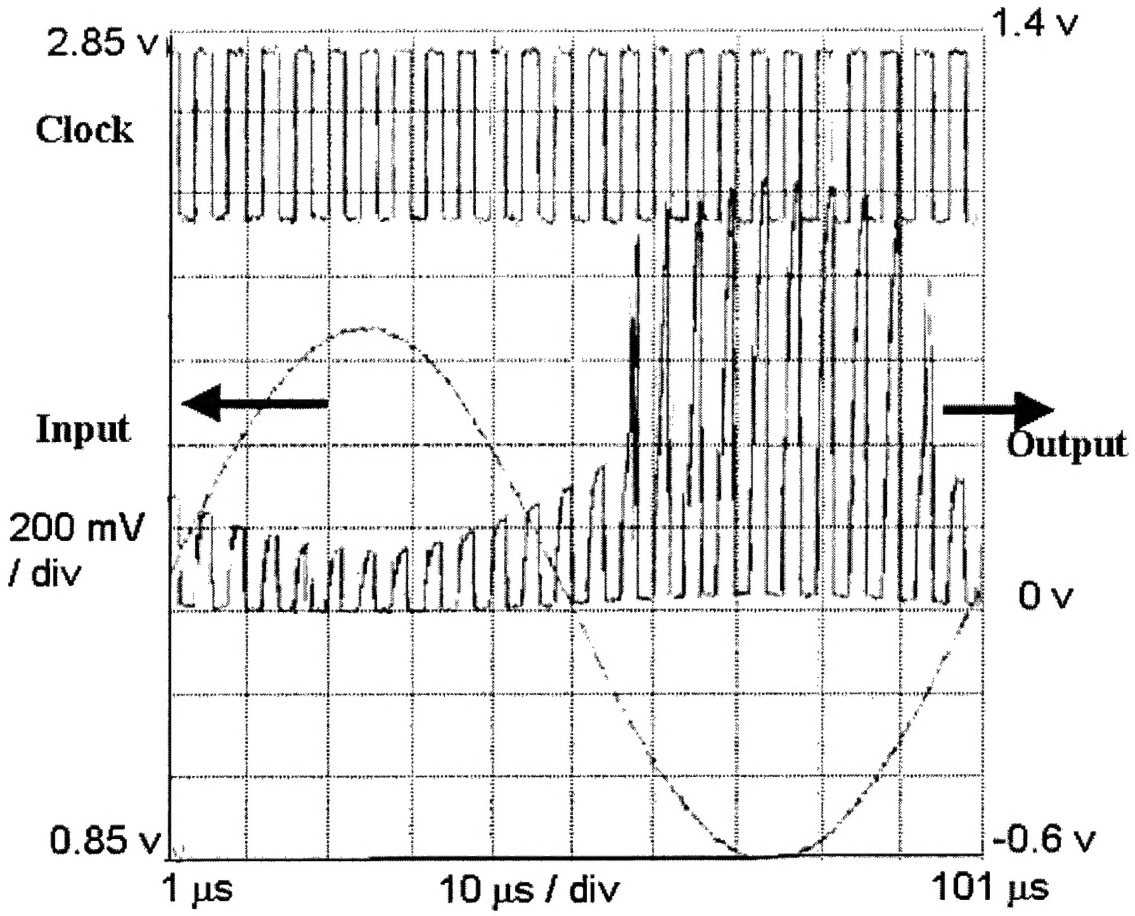
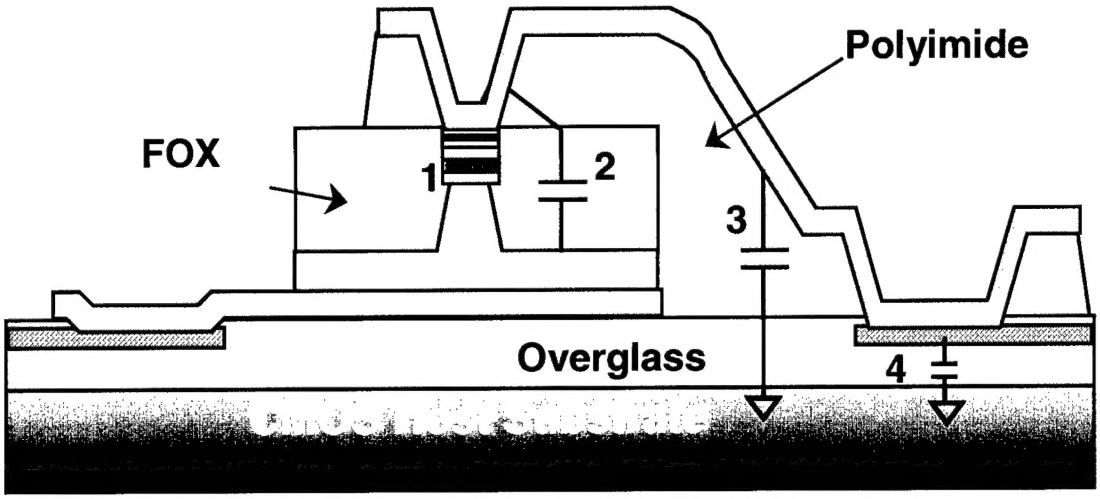
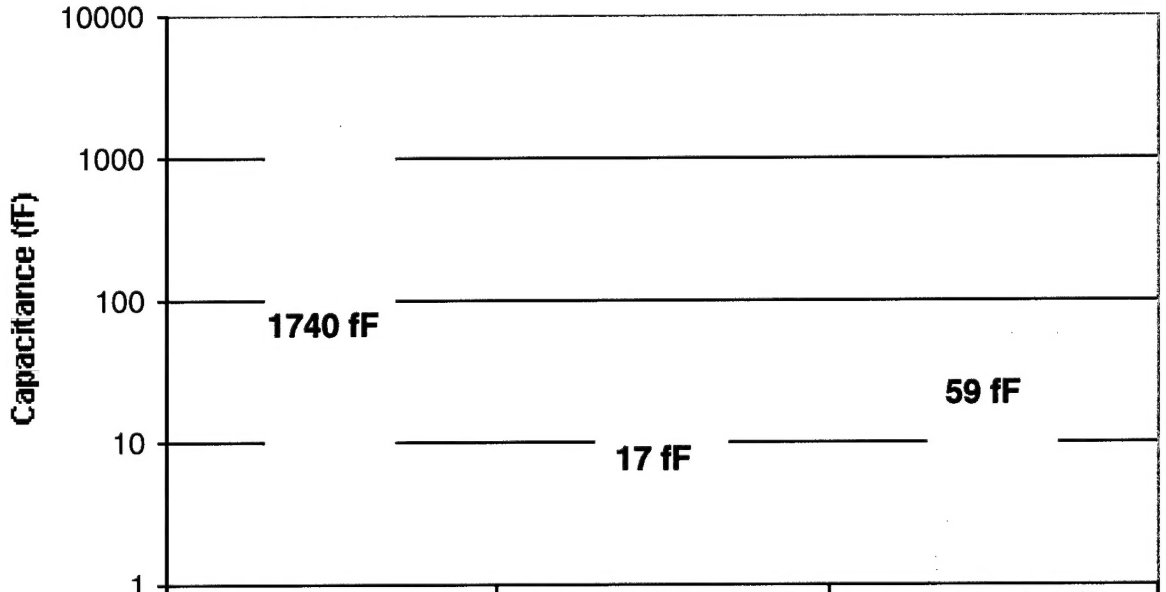


Figure 4. Transient operation of the RTD/CMOS comparator.



(a)



	Prototype 4x4 (fF)	Optimized 1.4x1.4 (fF)	Optimized 4x4 (fF)
4) CMOS Pad	16	4	4
3) Interconnect	20	2.9	2.9
2) Dielectric	1656	4.4	4.4
1) Device	48	6	48

(b)

Figure 5. The Distribution of the Parasitic Capacitance of a Thin-Film Integrated RTD. (a) There are four sources of parasitic capacitance associated with the integrated RTD: (1) the device capacitance of the RTD, (2) the parallel plate capacitance through the dielectric of the transferred RTD die, (3) interconnect capacitance, and (4) pad capacitance of the aluminum pad. (b) The overall parasitics of the fabricated prototype and the optimized structure illustrated in (a). The estimated total capacitance of the optimized structure is dominated by the device capacitance for RTDs above 2 × 2 μm.